Universiti Tun Hussein Onn Malaysia

UNIVERSITI TUN HUSSEIN ONN MALAYSIA

FINAL EXAMINATION
(TAKE HOME)
SEMESTER II
SESSION 2020/2021

COURSE NAME	:	VLSI SYSTEM / VLSI DESIGN
COURSE CODE	:	BEJ 43103 / BED 30303
PROGRAMME CODE	:	BEJ
EXAMINATION DATE	:	JULY 2021
DURATION	:	4 HOURS
INSTRUCTION	:	ANSWER **ALL** QUESTIONS. PLEASE UPLOAD YOUR ANSWER IN PDF FORM TO AUTHOR (UTHM LMS) WITHIN THE SPECIFIED TIME GIVEN.

THIS QUESTION PAPER CONSISTS OF **SIX (6)** PAGES

Q1 (a) Discuss the term 'Beyond CMOS' and relate it to the Moore's Law.

(5 marks)

(b) (i) Analyse a NOR CMOS dynamic logic circuit and demonstrate how a contention problem can occur in the circuit.

(6 marks)

(ii) Propose and explain a solution to eliminate the contention problem in the NOR circuit in **Q1(b)(i)**.

(4 marks)

(c) (i) State the monotonicity requirement in the CMOS dynamic logic circuits.

(2 marks)

(ii) Explain with suitable diagram the violation of monotonicity requirement in the CMOS dynamic logic circuits.

(3 marks)

Q2 Given the following Boolean equation:

$$Y = \overline{A\,E + B(CG + D + F)}$$

(a) Draw the fully complementary static CMOS logic circuit that represent the equation using minimum number of transistors.

(8 marks)

(b) Design a stick diagram for the equation that will produce the most compact layout.

(12 marks)

Q3 (a) (i) List **TWO (2)** sources of leakage current in CMOS transistor.

(2 marks)

(ii) Describe the reason why leakage current increases with the advancement of technology scaling in CMOS transistor.

(4 marks)

(b) A CMOS circuit is shown in **Figure Q3(b)**. The circuit should have an equivalent driving capability of an inverter. The minimum length for each transistor in the circuit is 2λ and the electron mobility is three (3) times faster than the mobility of hole.

(i) Determine the size of each transistor in the circuit to fulfil the stated requirement.

(9 marks)

(ii) Calculate the parasitic delay for the circuit and justify whether the calculated parasitic delay is the minimum value.

(5 marks)

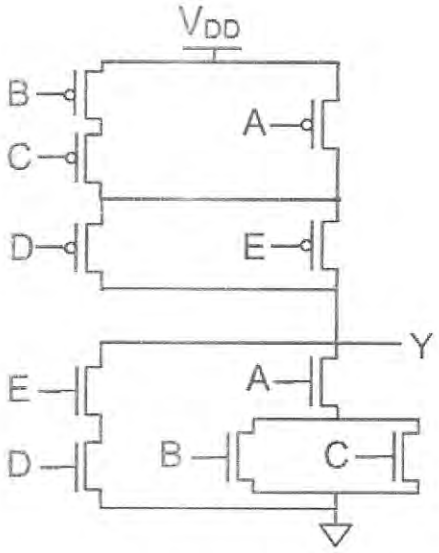

Figure Q3(b)

Q4 (a) Define a hold time for a falling edge triggered flip-flop. Clearly illustrate the hold time using a timing diagram.

(4 marks)

(b) (i) A D-latch is shown in **Figure Q4(b)(i)**. Determine the equation for Q of the D-latch.

(2 marks)

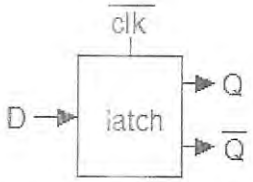

Figure Q4(b)(i)

(ii) Draw the circuit inside the D-latch using multiplexer and inverter.

(4 marks)

(c) Construct a negative edge D-flip-flop circuit and draw the circuit fully at transistor level.

(10 marks)

Q5 (a) **Figure Q5(a)** is a block diagram of a 1-to-4 demultiplexer.

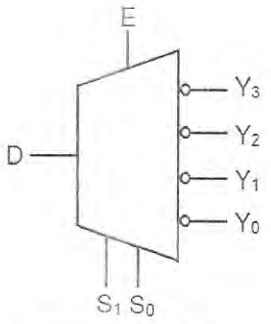

Figure Q5(a)

(i) Construct a truth table to show the relationship between the data input (D), enable input (E), the select line (S_1 and S_0) and the output (Y_0 to Y_3).

(5 marks)

(ii) Determine the equation for the output Y_n.
(Note: Each student will be assigned to a different output)

(4 marks)

(iii) Design the demultiplexer at transistor level with minimum number of transistors using pseudo-nMOS method by showing the circuit for Y_n. Clearly label the designed circuit. Assume all the inverted form of the inputs are available.

(5 marks)

(b) (i) Discuss about controllability and observability, the key concept in Design for Testability (DFT) for integrated circuit (IC).

(4 marks)

(ii) Explain Built-In Self Test (BIST) in Design for Testability (DFT) for integrated circuit (IC).

(2 marks)

– END OF QUESTIONS –