Universiti Tun Hussein Onn Malaysia

UNIVERSITI TUN HUSSEIN ONN MALAYSIA

FINAL EXAMINATION
SEMESTER I
SESSION 2021/2022

COURSE NAME	:	ELECTRONIC
COURSE CODE	:	DAE 21303
PROGRAMME CODE	:	DAE
EXAMINATION DATE	:	JANUARY/ FEBRUARY 2022
DURATION	:	6 HOURS
INSTRUCTION	:	1. ANSWER **ALL** QUESTIONS
		2. THIS FINAL EXAMINATION IS A **TAKE HOME** ASSESSMENT AND CONDUCTED VIA **OPEN BOOK**.

THIS QUESTION PAPER CONSISTS OF **SEVEN (7)** PAGES

Q1 (a) Sketch V_o in relation to input signal in **Figure Q1 (a)** for at least one complete cycle. Use second approximation model and assume zener voltage for D_1 and D_2 are 3.3 V.

(5 marks)

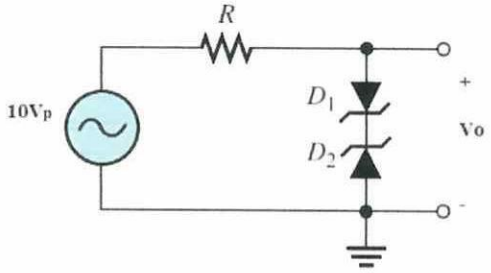

Figure Q1 (a)

(b) Design a clamper circuit that gives a steady state input and output as shown in **Figure Q1(b)**. Draw the corresponding circuit with all the components labelled. Show overall analysis to justify the proposed design.

(5 marks)

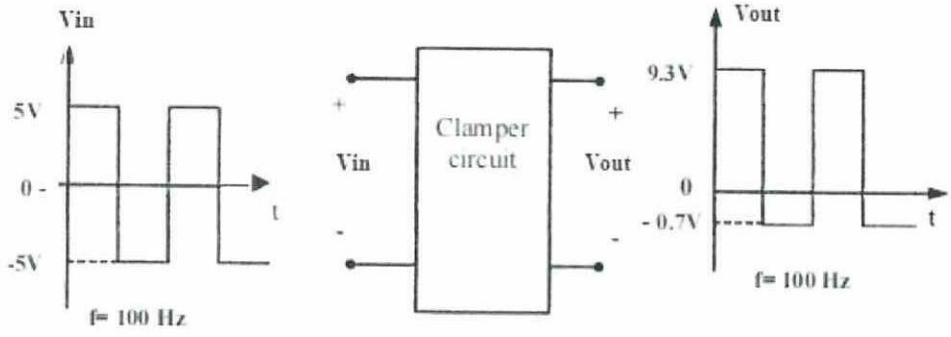

Figure Q1 (b)

(c) **Figure Q1(c)** shows a rectifier circuit connected to a filter capacitor and a zener diode, D_1. Given that I_{zmax} = 60 mA and I_{zmin} = 3 mA. From the circuit, determine the following parameters:

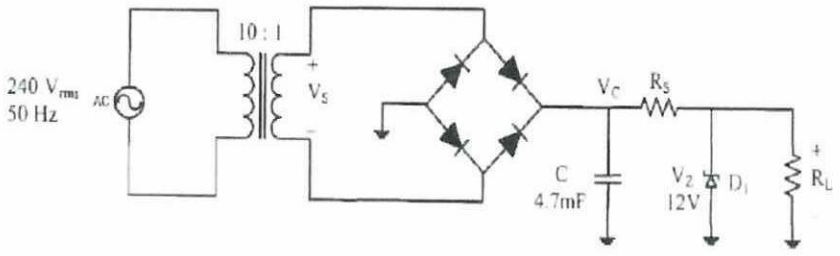

Figure Q1 (c)

(i) Sketch V_c with respect to the input signal, V_s.

(2 marks)

(ii) Average value of V_c if $V_{r(p\text{-}p)} = 2$ V.

(2 marks)

(iii) The range of R_s if 500 Ω ≤ R_L ≤ 1 k Ω.

(6 marks)

Q2 (a) The output waveform from a capacitive filter in an unregulated DC power supply is shown in **Figure Q2 (a)**. The AC line voltage is 230 V, 50 Hz and the diode forward voltage drop is 0.7 V. A center-tapped full wave rectifier is used and a load of 10 kΩ is connected across the capacitor.

(i) Draw the complete circuit

(3 marks)

(ii) Determine the value of the capacitor used.

(6 marks)

(iii) Find the transformer turns ratio, $N_p : N_s$

(4 marks)

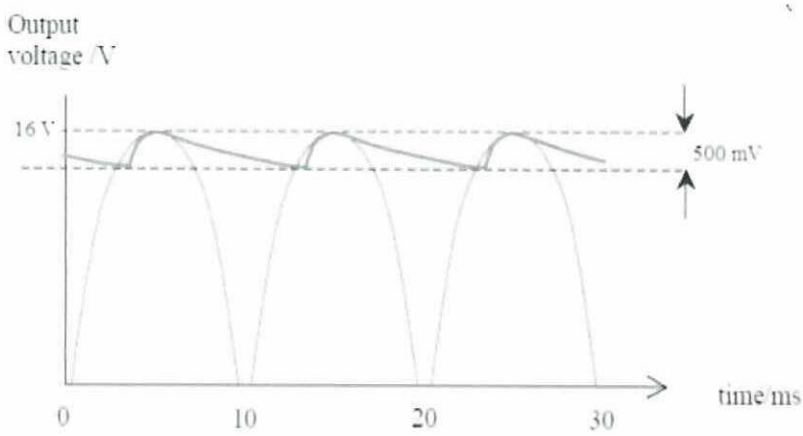

Figure Q2 (a)

(b) The circuit in **Figure Q2(b)** is used to drive an electrical appliance, represented by a load, R_L. For the zener diode, its breakdown voltage is 8.2 V. The voltage of unregulated power supply, V_o is 15 V.

(i) Calculate the current across zener diode, I_Z.

(3 marks)

(ii) Calculate the zener power and power dissipation by R_L.

(4 marks)

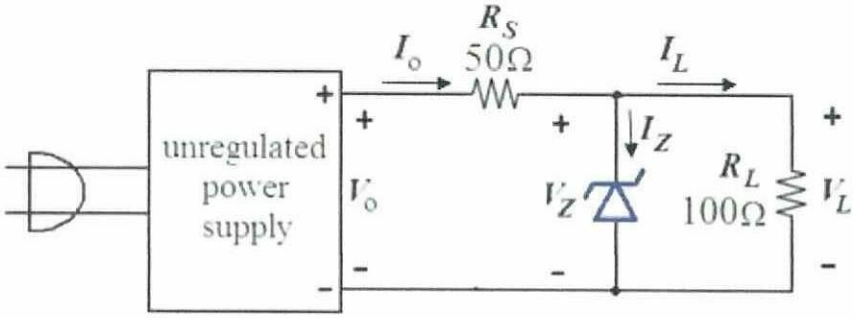

Figure Q2 (b)

Q3 Refer the amplifier network in **Figure Q3**.

(a) Determine base current, I_B and collector current, Ic.

(6 marks)

(b) Determine emitter voltage, V_E and collector-to-emitter voltage, V_{CE}.

(3 marks)

(c) Draw the DC load line. Label $I_{c(sat)}$, $V_{CE(cutoff)}$, and the Q-points.

(4 marks)

(d) Sketch the AC equivalent circuit using r_e model and determine the AC dynamic resistance, r_e.

(3 marks)

(e) Determine the input impedance, Z_i, output impedance, Z_o and the voltage gain, A_v for the circuit.

(4 marks)

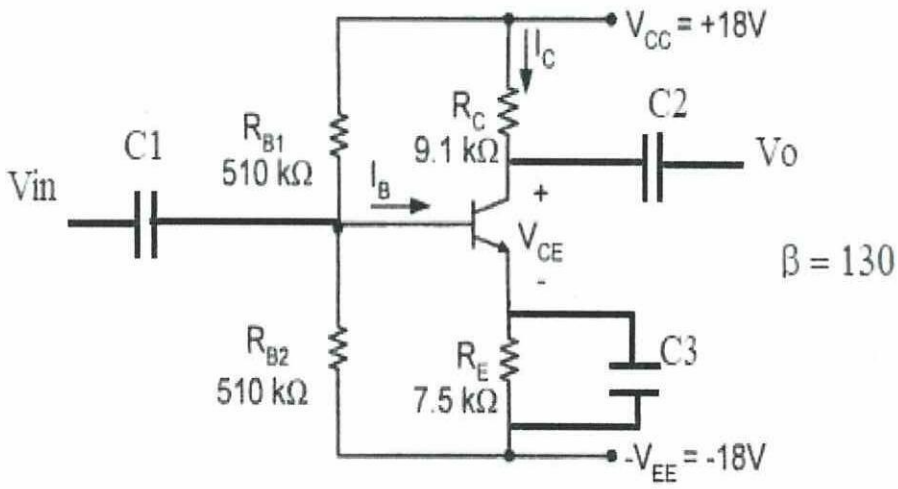

Figure Q3

Q4 (a) For the JFET Voltage - Divider biasing of **Figure Q4(a)**, given $I_{DSS} = 9$ mA and $V_P = -3$ V, determine the following if given Shockley's equation:

$$I_D = I_{DSS}\left(1 - \frac{V_{GSQ}}{V_P}\right)$$

(i) Gate voltage, V_G. (1 marks)

(ii) Q-Operating point; I_{DQ} and V_{GSQ}. (8 marks)

(iii) Drain-to-source voltage, V_{DSQ}. (1 marks)

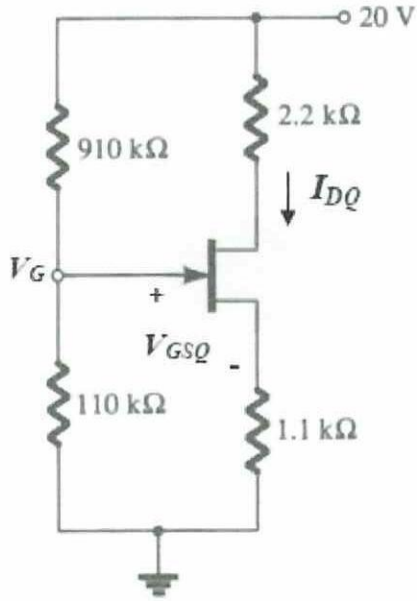

Figure Q4 (a)

(b) The JFET Self-Bias common-source amplifier in **Figure Q4(b)** will produce a voltage gain of **10**. The device should be biased at V_{GSQ} = **1/3 (V_P)**. Determine the following if I_{DSS} = 8 mA, V_P = -4V, r_d = 40 kΩ and given;

$$g_m = \frac{2I_{DSS}}{|V_P|}\left(1 - \frac{V_{GSQ}}{V_P}\right)$$

(i) R_D and R_S

(7 marks)

(ii) Input impedance, Z_i and output impedance, Z_o

(3 marks)

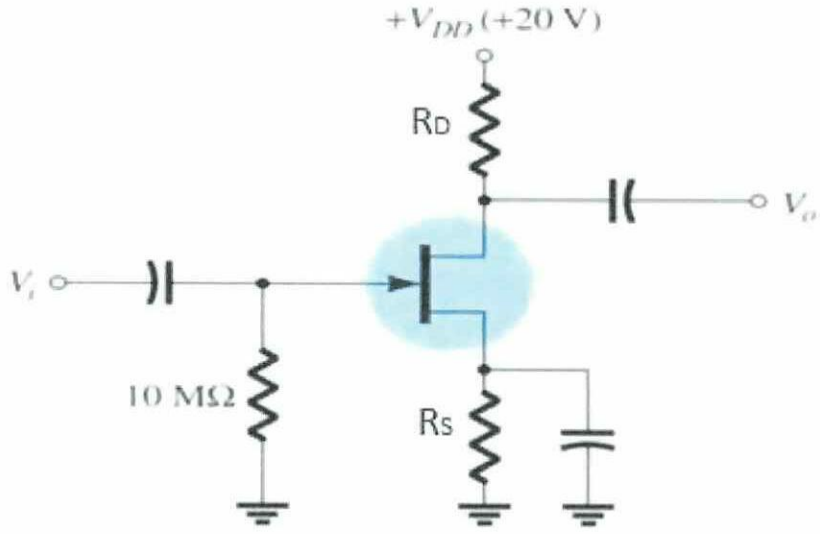

Figure Q4 (b)

- END OF QUESTION-