Universiti Tun Hussein Onn Malaysia

UNIVERSITI TUN HUSSEIN ONN MALAYSIA

FINAL EXAMINATION
SEMESTER I
SESSION 2021/2022

COURSE NAME	:	DIGITAL ELECTRONICS
COURSE CODE	:	DAE 21203
PROGRAMME CODE	:	DAE
EXAMINATION DATE	:	JANUARY / FEBRUARY 2022
DURATION	:	2 HOURS 30 MINUTES
INSTRUCTION	:	1. ANSWER **ALL** QUESTIONS. 2. THIS FINAL EXAMINATION IS A **ONLINE** ASSESSMENT AND CONDUCTED VIA **OPEN BOOK**.

THIS QUESTION PAPER CONSISTS OF **SIXTEEN (16)** PAGES

PART A: ANSWER ALL QUESTIONS IN THE ANSWER SHEET

(1 mark each)

Q1 A quantity that has continuous values is

A. a digital quantity
B. a binary quantity
C. an analog quantity
D. a natural quantity

Q2 Which of the following is not an advantage of digital system?

A. Less affected by noise
B. Operation can be programmed
C. Energy usage is minimal
D. Information storage is easy

Q3 The term *bit* means

A. a small amount of data
B. binary digit
C. a "1" or "0"
D. both answers B and C

Q4 How much time is required for a parallel transfer of 16 bits data if the clock frequency is 100 MHz?

A. 10 ms
B. 16 µs
C. 1 µs
D. 10 ns

Q5 Which quantity below representing an analog quantity?

A. the hourly changes of air temperature
B. vehicle speed over an hour
C. original sound wave
D. recorded data on CD tracks

Q6 Convert binary 111011110010_2 to hexadecimal.

A. $EF2_{16}$
B. $FF2_{16}$
C. $FE2_{16}$
D. $FD2_{16}$

Q7 Convert binary 010111100_2 numbers to octal.

A. 172_8
B. 272_8
C. 174_8
D. 274_8

Q8 Identify gate X based on the waveform in the **Figure Q8**.

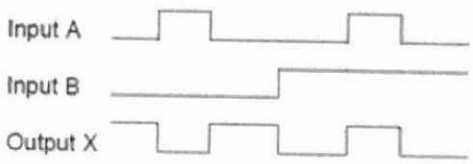


Figure Q8

A. AND
B. XNOR
C. NAND
D. XOR

Q9 Find the Boolean expression for the combinational logic circuit in the **Figure Q9**.

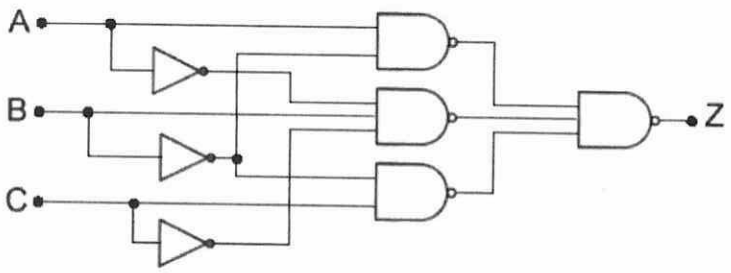


Figure Q9

A. $Z = \overline{(A\bar{B})} \bullet \overline{(\bar{A}B\bar{C})} \bullet \overline{(\bar{B}C)}$

B. $Z = (A\bar{B}) \bullet (\bar{A}B\bar{C}) \bullet (\bar{B}C)$

C. $Z = \overline{(A\bar{B})} + \overline{(AB\bar{C})} + \overline{(BC)}$

D. $Z = \overline{(A\bar{B})} \bullet \overline{(AB\bar{C})} \bullet \overline{(\bar{B}C)}$

Q10 A 5 variable Karnaugh map contains

A. 16 cells
B. 32 cells
C. 64 cells
D. 25 cells

Q11 On a Karnaugh map, grouping the 0s produces

A. a POS expression
B. a "don't care" condition
C. a SOP expression
D. AND-OR logic

Q12 Which one is NOT a valid rule for Boolean algebra?

A. $A+1 = 1$
B. $A \bullet A = A$
C. $A \bullet 1 = A$
D. $A+1 = A$

Q13 $A(A + B) = ?$

A. AB
B. 1
C. $(1+AB)$
D. A

Q14 The AND operation can be produced with

A. two NAND gates
B. one NOR gate
C. three NAND gates
D. three OR gates

Q15 The expression $\bar{A}BCD + ABC\bar{D} + A\bar{B}\bar{C}D$

A. cannot be simplified
B. is simplified to $\bar{A}BC + A\bar{B}$
C. is simplified to $ABC\bar{D} + \bar{A}B\bar{C}$
D. None of the answers is correct

Q16 Which of the following input and output value are **incorrect** for the 4-bit parallel binary adder/subtractor circuit in the **Figure Q16**?

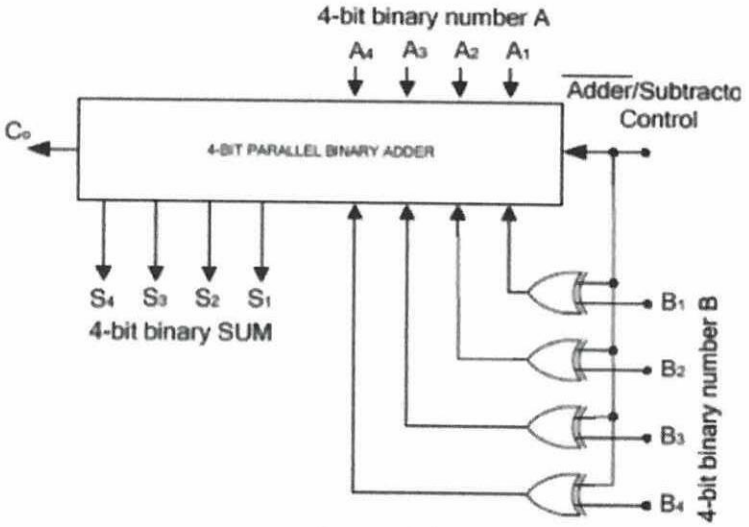


Figure Q16

	[A]	[B]	$\overline{\text{Adder/Subtractor}}$	Cout	[Σ]
A.	1101	0110	0	1	0011
B.	1001	1000	0	1	0001
C.	1111	1011	1	0	0100
D.	0101	1000	1	0	1011

Q17 Data selectors are basically the same as

A. decoders
B. demultiplexers
C. multiplexers
D. encoders

Q18 Determine the summation of this binary: 101101+01011

A. 011010
B. 1010100
C. 101110
D. 1001000

Q19 An example of a SOP expression is

A. $A+B(C+D)$
B. $(A+B+C)(\bar{A}+B+C)$
C. $\bar{A}B+AC+\bar{A}BC$
D. Both answers A and B

Q20 Add the two BCD numbers: 1001 + 0100

A. 1101
B. 00001101
C. 00010011
D. 00110001

Q21 The device shown in the **Figure Q21** is most likely a _____

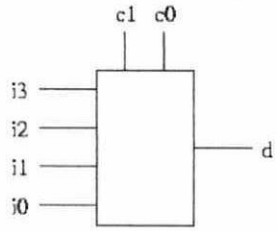


Figure Q21

A. Comparator
B. Multiplexer
C. Inverter
D. Demultiplexer

Q22 To expand a 4 bit parallel adder to an 8 bit parallel adder you must

A. use 4 bit adders with no connections.
B. use eight 4 bit adders with no interconnections.
C. use two 4 bit adders and connect to the sum outputs of one to the bit output of the other.
D. use two 4 bit adders with the carry output of one connected to the carry input of the other.

Q23 In 1-to-8 demultiplexer, how many select lines are required?

A. 2
B. 3
C. 4
D. 5

Q24 If a 74LS85 magnitude comparator has A = 1011 and B = 1001 on the inputs, the outputs are:

A. A>B = 0, A<B = 1, A=B = 0
B. A>B = 1, A<B = 1, A=B = 0
C. A>B = 1, A<B = 0, A=B = 0
D. A>B = 0, A<B = 0, A=B = 1

Q25 The full-adder shown by the **Figure Q25** is tested under all input conditions with the input waveforms shown. From your observation of the SUM and COUT waveforms, is it operating properly, and if not, what is the most likely fault?

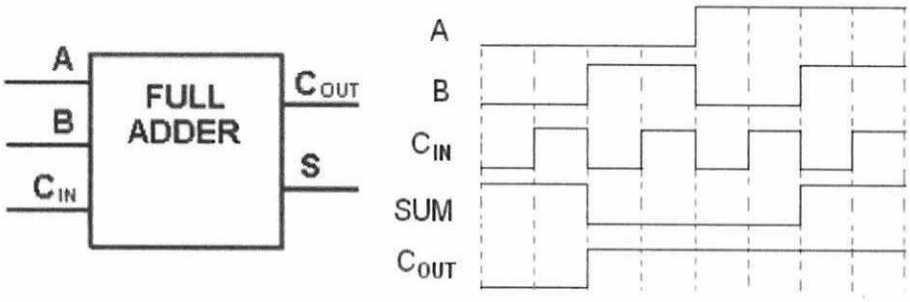


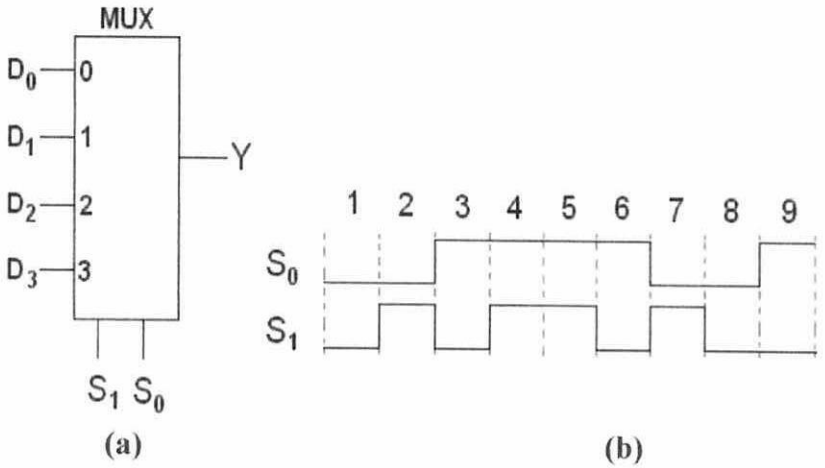
Figure Q25

A. Yes, the output SUM and COUT are correct.
B. No, the input B is accidentally connected to VCC.
C. No, the input CIN is accidentally connected to VCC.
D. No, the input A is accidentally connected to VCC.

Q26 Table shown is a truth table for a 4-to-2 line priority encoder. Determine the correct combination of inputs and outputs.

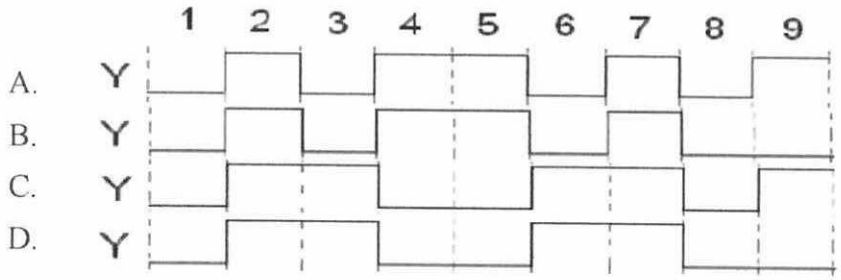
	Inputs					Outputs	
	En	D0	D1	D2	D3	A1	A0
A.	0	0	0	0	1	x	x
B.	1	1	0	0	1	0	0
C.	1	0	1	0	1	0	1
D.	1	0	0	1	1	1	1

Q27 The following data input has been applied to the multiplexer shown in **Figure Q27(a)**: D_0=0, D_1=1, D_2=1, and D_3=0. The data-select inputs to the multiplexer are sequenced as shown by the waveforms in **Figure Q27(b)**, determine the output waveform.



(a) **(b)**

Figure Q27



Q28 What is the combinational logic circuit in the **Figure Q28** represent?

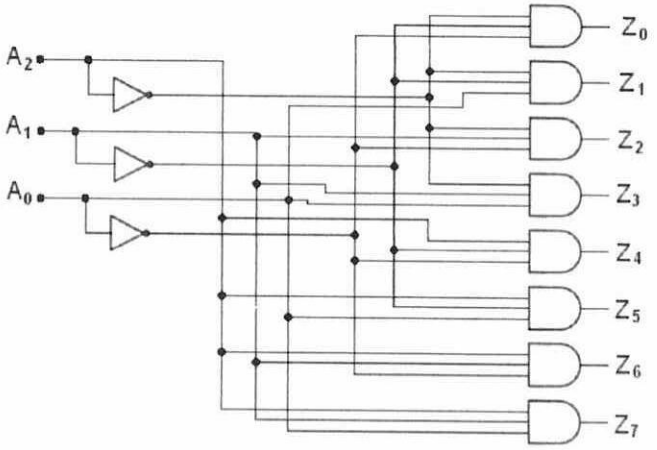


Figure Q28

A. 3-to-8 decoder
B. BCD-to-7 segment decoder
C. 3-to-8 encoder
D. 8-to-3 encoder

Q29 2's complement of 1011101 is

A. 0101110
B. 1001101
C. 0100010
D. 0100011

Q30 Serial data transmission is employed to send data from a computer to a modem. The least significant bit is sent first. What is the data received at the modem if the data is 01001110?

A. 01001110
B. 01100010
C. 01110010
D. 01011110

Q31 A _____ is a combinational circuit element that selects data from one of many inputs and directs it to a single output.

A. encoder
B. decoder
C. multiplexer
D. demultiplexer

Q32 Convert the following binary number into gray code: 100101_2

A. 101101_{GRAY}
B. 001110_{GRAY}
C. 110111_{GRAY}
D. 111001_{GRAY}

Q33 In a 4 variable Karnaugh map , a 2- variable a product term is produced by grouping

A. two adjacent cells of bit 1s
B. two adjacent cells of bit 0s
C. four adjacent cells of bit 1s
D. eight adjacent cells of bit 1s

Q34 In 1-to-4 demultiplexer, if S1 = 1 & S2 = 1, then the output will be

A. *Z0*
B. *Z1*
C. *Z2*
D. *Z3*

Q35 How many inputs will a decimal-to-BCD encoder have?

A. 4
B. 8
C. 10
D. 16

Q36 How many outputs will a decimal-to-BCD encoder have?

A. 4
B. 8
C. 10
D. 16

Q37 How many VALID entries for an R-S flip-flop?

A. 1
B. 2
C. 3
D. 4

Q38 Which of the following is correct for a gated D-type flip-flop?

A. The Q output is either SET or RESET as soon as the D input goes HIGH or LOW
B. The output complement follows the input when enabled
C. Only one of the inputs can be HIGH at a time
D. The output toggles if one of the inputs is held HIGH

Q39 A counter circuit is usually constructed of _____

A. A number of latches connected in cascade form
B. A number of NAND gates connected in cascade form
C. A number of flip-flops connected in cascade
D. A number of NOR gates connected in cascade form

Q40 BCD counter is also known as _____

A. Parallel counter
B. Decade counter
C. Synchronous counter
D. Asynchronous counter

PART A: ANSWER SHEET

Q1		Q21	
Q2		Q22	
Q3		Q23	
Q4		Q24	
Q5		Q25	
Q6		Q26	
Q7		Q27	
Q8		Q28	
Q9		Q29	
Q10		Q30	
Q11		Q31	
Q12		Q32	
Q13		Q33	
Q14		Q34	
Q15		Q35	
Q16		Q36	
Q17		Q37	
Q18		Q38	
Q19		Q39	
Q20		Q40	

PART B: ANSWER ALL QUESTIONS

Q1 Given Boolean expression of:

$$Z = \bar{C} \cdot \overline{D} + A \cdot \overline{B} \cdot \overline{D} + \bar{A} \cdot B + A \cdot B \cdot D + B \cdot C$$

(a) Change the Boolean expression to its standard SOP form.

(4 marks)

ANSWER:

(b) Obtain the truth table for the logic circuit showing all inputs, A, B, C and D and output, Z.

(4 marks)

ANSWER:

(c) By using the Karnaugh map method shown in **Figure Q1(c)**, show that the Boolean expression can further be simplified.

(6 marks)

ANSWER:

Z	$\overline{C}$ $\overline{D}$	$\overline{C}$ D	C D	C $\overline{D}$
$\overline{A}$ $\overline{B}$				
$\overline{A}$ B				
A B				
A $\overline{B}$				

Figure Q1(c)

(d) Construct the circuit of simplified expression in **Q1(c)** with NAND gates only.

(6 marks)

ANSWER:

Q2 (a) Design a system with four inputs, P, Q, R and S, and one output, Z such that Z = 1 if three or more of the inputs are 0.

(i) Build the truth table for the system.

(4 marks)

ANSWER:

(ii) Construct the circuit of the system using 16-to-1 multiplexer

(6 marks)

ANSWER:

(b) Circuit in **Figure Q2(b)(i)** has three inputs (A, B and C) and one output (Z), connected to a decoder IC 74LS138 and NAND gate IC SN7420N. Construct and fill in the truth table shown in **Table Q2(b)** for the output, Z. Refer to **Figure Q2(b)(ii)** for datasheet pin assignment.

(10 marks)

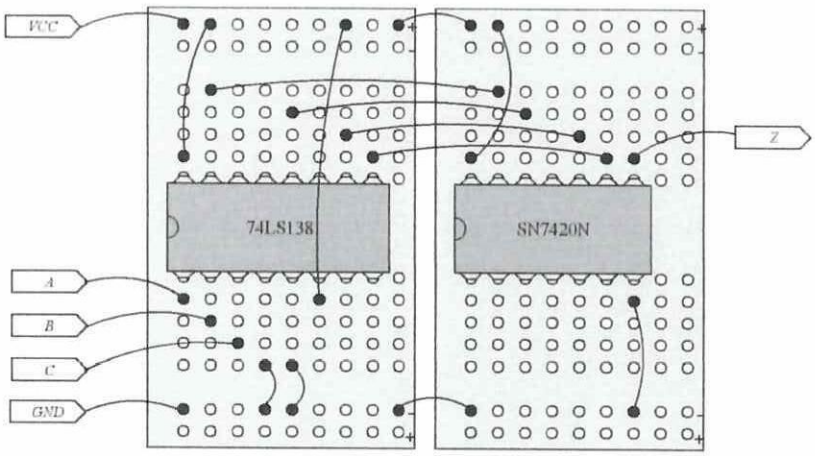


Figure Q2(b)(i)

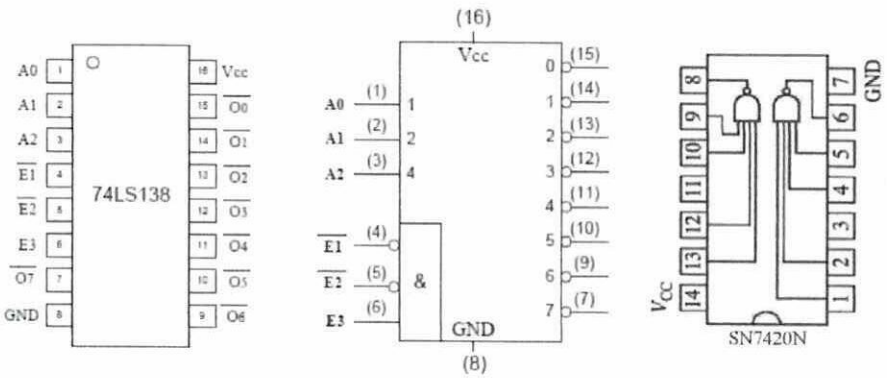


Figure Q2(b)(ii)

ANSWER:

Table Q2(b)

C	*B*	*A*	*Z*

Q3 (a) The waveforms for signals A and B shown in **Figure Q3(a)(i)** are applied to the circuit shown in **Figure Q3(b)(ii)**. Evaluate the waveforms for P, Q, R and S in the **Figure Q3(a)(iii)**. Assumes that initially R=0 and S=1.

(6 marks)

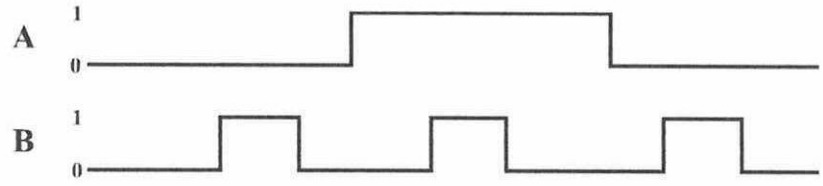


Figure Q3(a)(i)

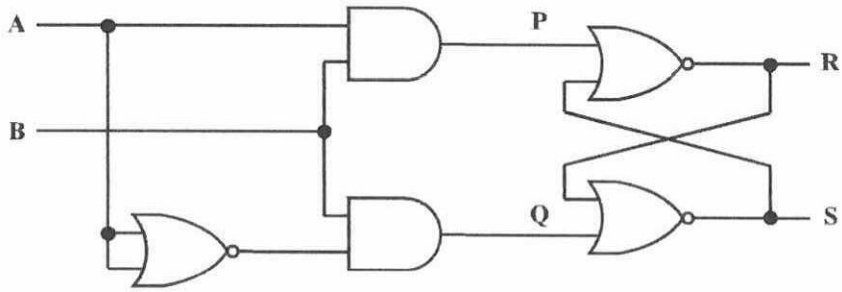


Figure Q3(a)(ii)

ANSWER:

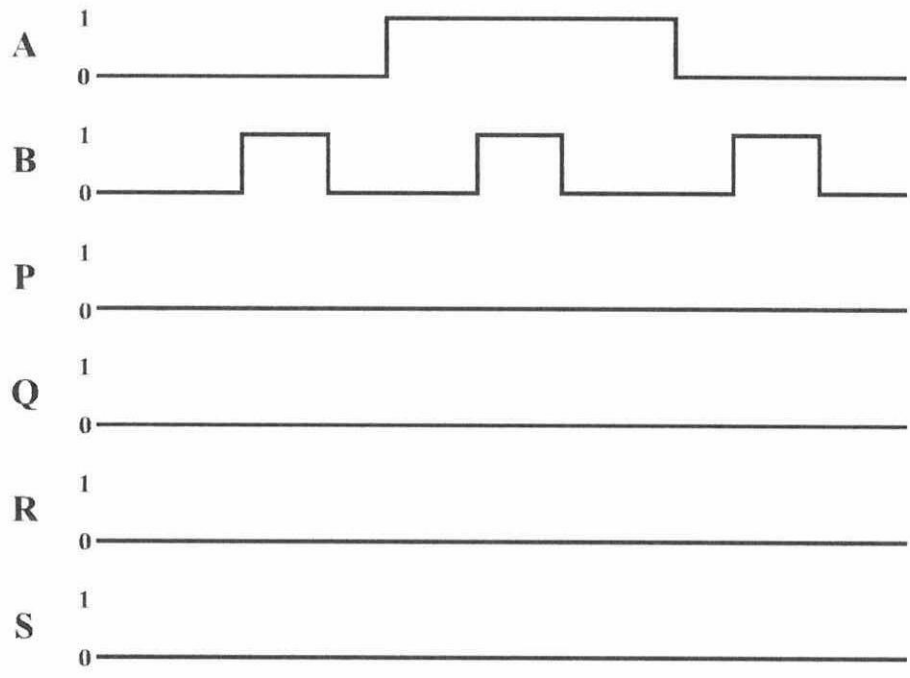


Figure Q3(a)(iii)

(b) Design a synchronous counter using JK flip-flop to count 4 digits number. The count sequence is 2,0,1,3 and repeat. The JK excitation table is shown in **Table Q3(b)**. Show all steps and the design should include the following :

Table Q3(b): JK FF's Excitation Table

Q(t)	Q(t+1)	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

(i) State diagram. (2marks)

ANSWER:

(ii) Excitation table. (4 marks)

ANSWER:

(iii) K-maps to generate minimal expression. (4 marks)

ANSWER:

(iv) Circuit implementation. (4 marks)

ANSWER:

- END OF QUESTIONS –