UNIVERSITI TUN HUSSEIN ONN MALAYSIA

FINAL EXAMINATION
SEMESTER I
SESSION 2014/2015

COURSE NAME	:	LOGIC SYSTEMS
COURSE CODE	:	DAE 21603
PROGRAMME	:	2 DAE
EXAMINATION DATE	:	DECEMBER 2014/ JANUARY 2015
DURATION	:	2 HOURS 30 MINUTES
INSTRUCTION	:	ANSWER **FOUR (4)** QUESTIONS ONLY

THIS QUESTION PAPER CONSISTS OF **NINE (9)** PAGES

Q1 (a) With the aid of truth tables, describe the dfferences between the following flip flops:

(i) RS flip flop
(ii) JK flip flop
(iii) D flip flop

(8 marks)

(b) Given J, K, Preset, Clear and Clock input for a JK flip-flop in **Figure Q1(b).**

(i) Draw the Q output waveform.
(ii) Explain the operation of this JK flip-flop.

(10 marks)

(c) For the circuit in **Figure Q1(c):**

(i) State the function of this circuit
(ii) Determine the external resistors R1 and R2 to give an output frequency of 10 kHz and duty cycle of 60% if the external capacitor C is 3 nF.

(7 marks)

Q2 (a) State the key difference between flip-flops and latches.

(3 marks)

(b) Connect 3 negative edge triggered JK Flip flops as an asynchronous count up counter. This flip-flop has an active low asynchronous clear input.

(i) Draw the circuit diagram
(ii) Draw the timing diagram (Use **Figure Q2(b)**) and show the count sequence.
(iii) Modify the circuit to operate as a MOD 6 counter.
(iv) If the input clock frequency is 2 kHz, determine the output frequency of the MOD 6 counter.

(11 marks)

(c) Design a synchronous counter using JK flip-flops to count 4 digits. The count sequence is 2,0,3,1 and repeat. The JK excitation table is shown in **Table Q2**. Show all steps and the design should include the following:

(i) State diagram
(ii) Circuit excitation table used to determine JK flip-flop inputs.
(iii) K-maps used to generate minimal expressions for JK inputs.
(iv) Logic circuit.

(11 marks)

Q3 (a) Show the following connections:

(i) Use JK flip-flops to divide a digital signal frequency by 8.
(ii) Use D-type flip-flops to divide a digital signal frequency by 4.

(6 marks)

(b) The logic diagram and Dual-In-Line Package for IC 7493 is given in **Figure Q3(b).** Draw the connections diagrams for the following 7493-based counters and determine the output frequency if the input clock frequency is 100 kHz. Show all steps and label the input clock as well as the outputs.

(i) MOD 8 counter
(ii) MOD 16 counter
(iii) MOD 11 counter.

(11 marks)

(c) Determine the maximum input clock frequency (f_{max}) for the counter shown in **Figure Q3(c)** if the propagation delay, t_{pd} for each flip-flop is 50 ns and t_{pd} for AND gate is 20 ns. Compare this with a MOD-16 ripple counter.

(8 marks)

Q4 (a) Determine the number of flip-flops needed to construct a shift register capable of storing:

(i) a 5-bit binary number
(ii) decimal numbers up to 32
(iii) hexadecimal numbers up to E.

(5 marks)

(b) With the aid of logic circuits and tables showing the sequence of states, describe the differences between a Ring counter and a Johnson counter.

(12 marks)

(c) **Figure Q4(c)** shows a bidirectional shift register. The serial input (IN) is LOW. Assume that initially outputs $Q_0Q_1Q_2Q_3 = 1010$. Do the following if RIGHT/$\overline{LEFT}$ input is held HIGH.

(i) Analyze **two (2)** of the combinational logic circuit outputs to determine how the output of each flip-flop is connected. Show all steps.
(ii) Redraw the 4 flip-flops (without showing the combinational circuits) indicating the correct shift.

(8 marks)

Q5 (a) Describe **five (5)** basic steps taken to create and load a digital circuit into a PLD?

(5 marks)

(b) Name **three (3)** advantages of constructing a digital circuit prototype using a PLD instead of standard logic devices.

(3 marks)

(c) Several types of architecture are used in PLDs. Draw the block diagram of three common types and describe their differences.

(6 marks)

(d) Use the PLA in **Figure Q5(d)** to implement the following functions. Label all inputs and outputs.

(i) $F1(W,X,Y) = \sum(1,2,3,5,7)$
(ii) $F2(W,X,Y) = \sum(0,4,6,7)$

(11 marks)

Q6 (a) **Figure Q6(a)** shows a simplified view of a typical computer system.

(i) Describe the semiconductor memory devices used.
(ii) Explain the differences between the **three (3)** storage devices based on the technology each uses.
(iii) Describe the functions of the **three (3)** buses shown.

(13 marks)

(b) A certain memory has a capacity of 4K x 8, determine

(i) the number of data inputs and data outputs .
(ii) the number of address lines.
(iii) its capacity in bytes.

(6 marks)

(c) List and describe the **three (3)** major operations in a flash memory.

(6 marks)

- END OF QUESTION –

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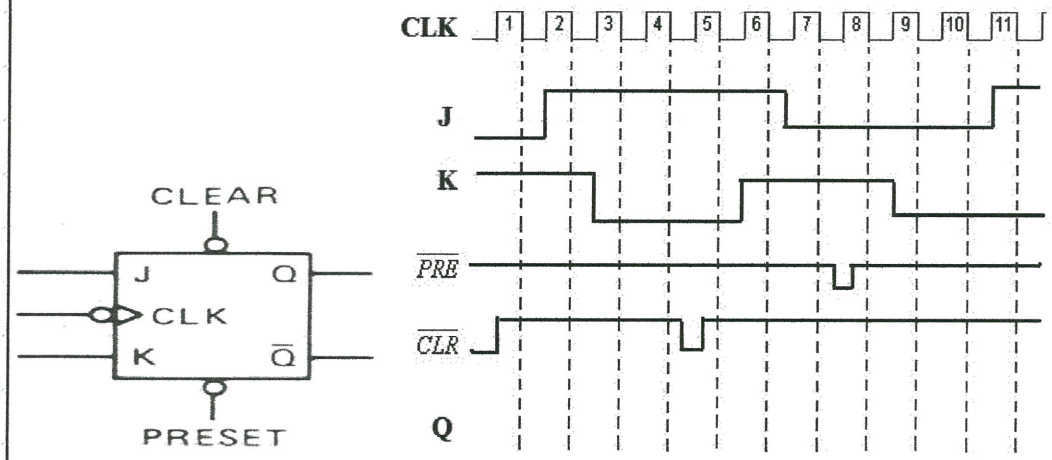

FIGURE Q1(b)

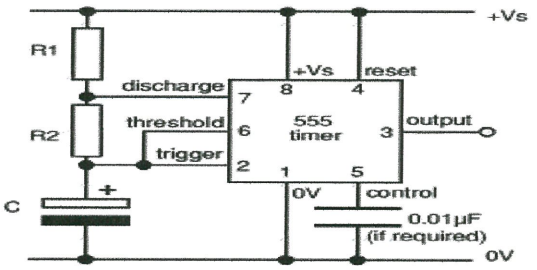

FIGURE Q1(c)

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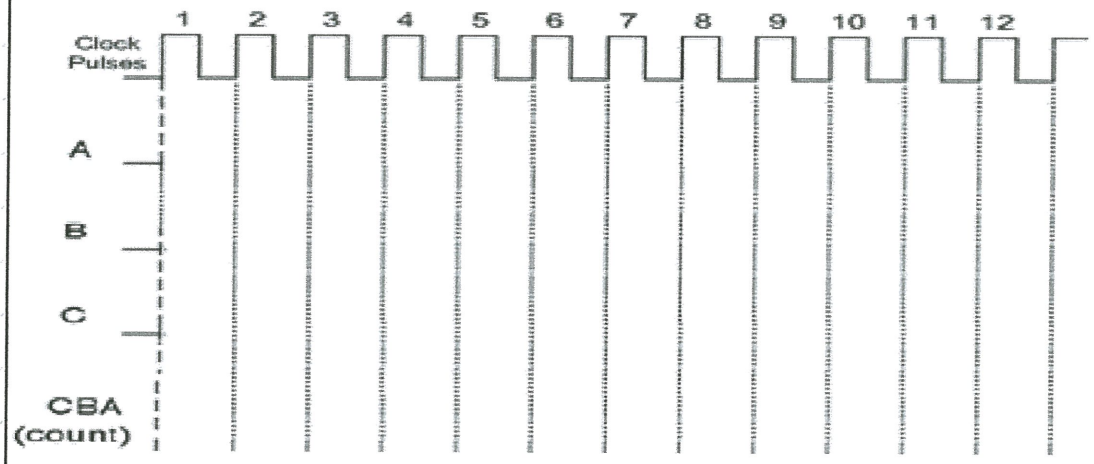

FIGURE Q2(b)

TABLE Q2: JK Excitation Table

Q(t)	Q(t+1)	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

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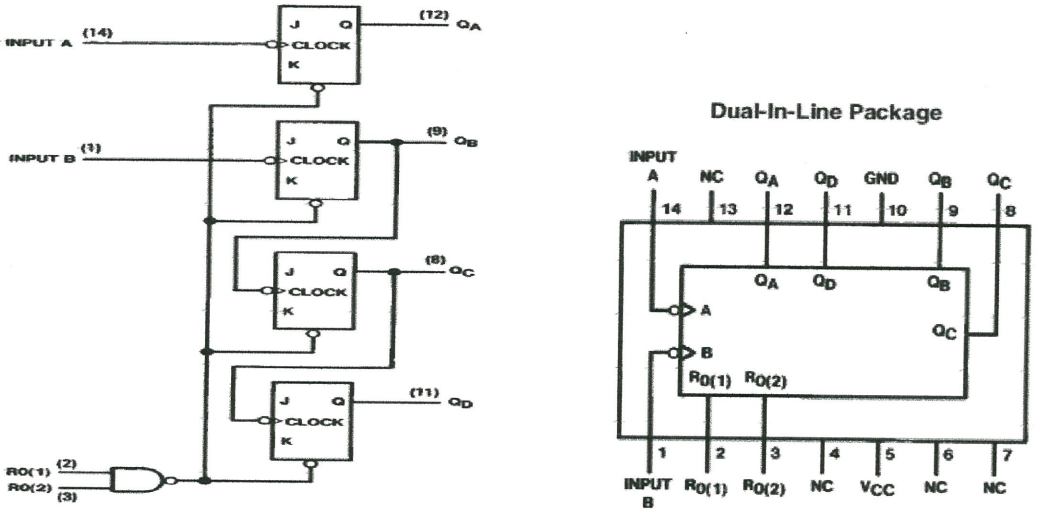

FIGURE Q3(b)

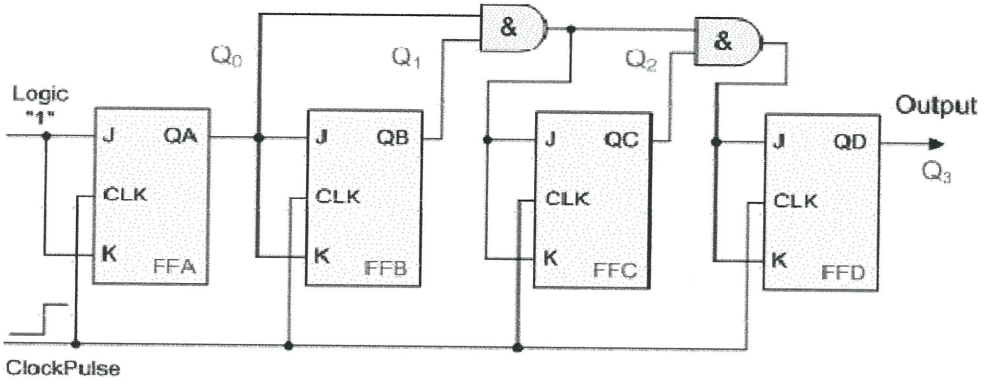

FIGURE Q3(c)

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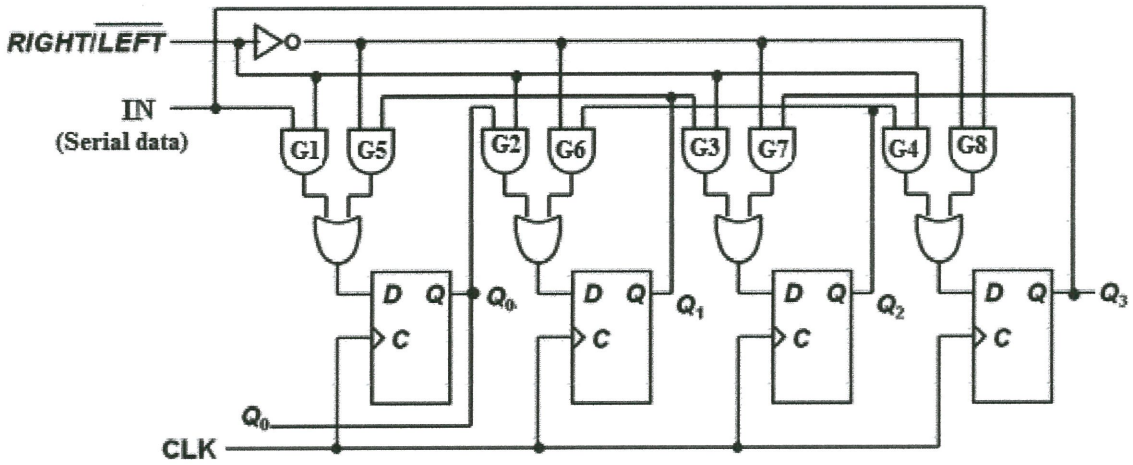

FIGURE Q4(c)

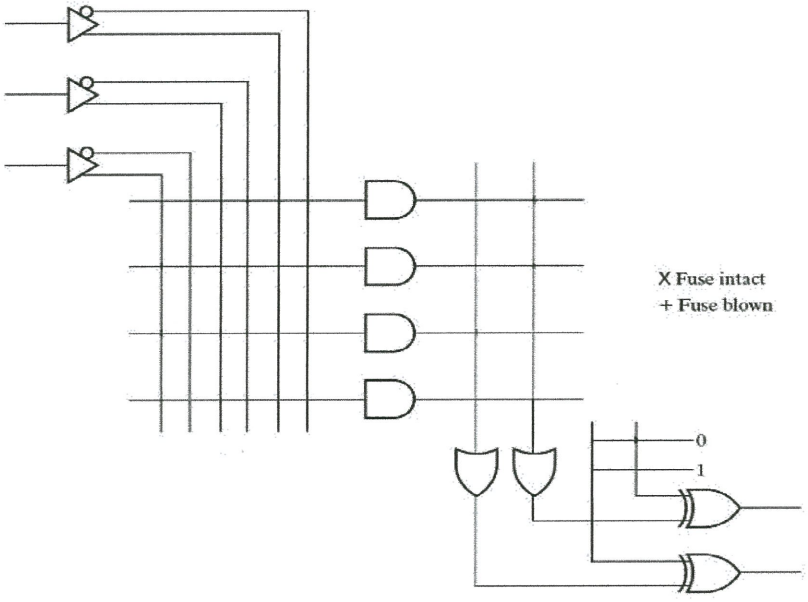

FIGURE Q5(d)

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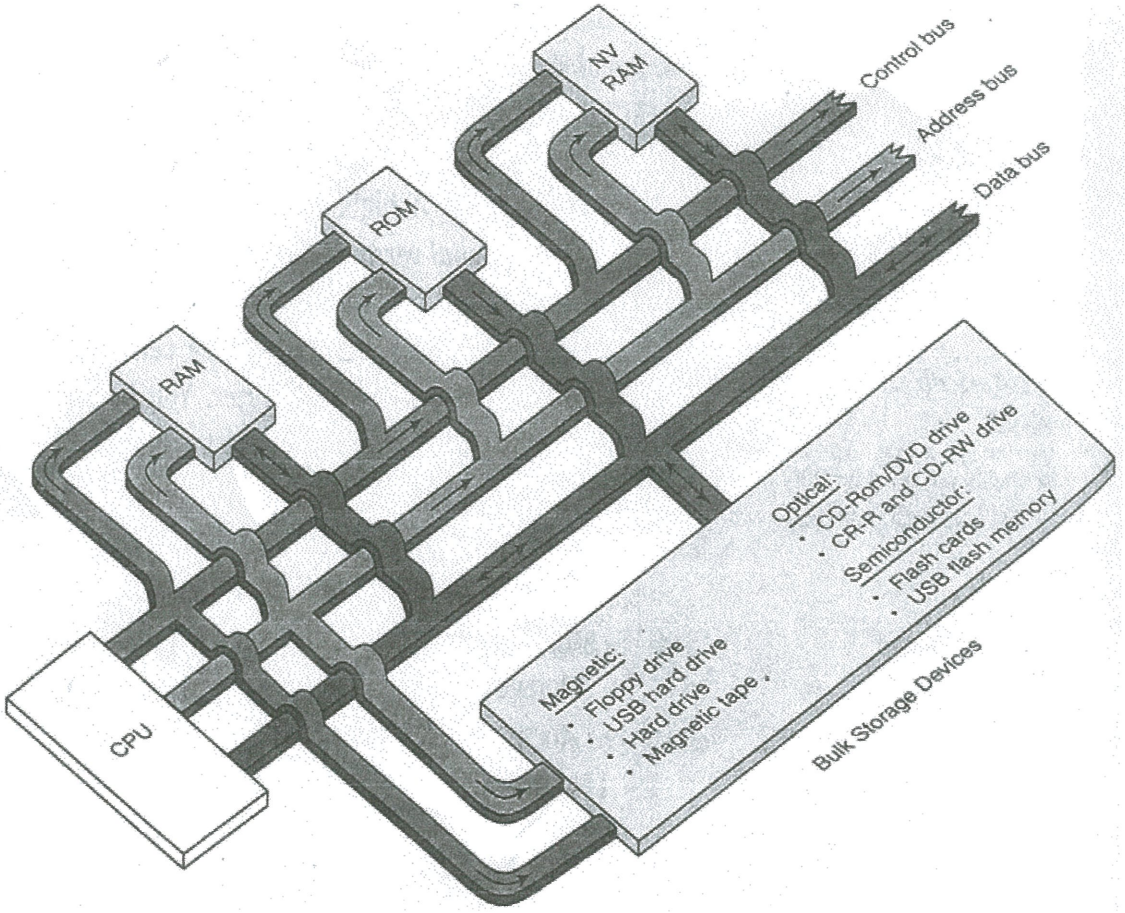

FIGURE Q6(a)