UTHM
Universiti Tun Hussein Onn Malaysia

UNIVERSITI TUN HUSSEIN ONN MALAYSIA

FINAL EXAMINATION
SEMESTER II
SESSION 2022/2023

COURSE NAME	:	DIGITAL DESIGN
COURSE CODE	:	BEJ 30503
PROGRAMME CODE	:	BEJ
EXAMINATION DATE	:	JULY / AUGUST 2023
DURATION	:	3 HOURS
INSTRUCTION	:	1. ANSWER **ALL** QUESTIONS
		2. THIS FINAL EXAMINATION IS CONDUCTED VIA **CLOSED BOOK.**
		3. STUDENTS ARE **PROHIBITED** TO CONSULT THEIR OWN MATERIAL OR ANY EXTERNAL RESOURCES DURING THE EXAMINATION CONDUCTED VIA CLOSED BOOK

THIS QUESTION PAPER CONSISTS OF **SIX (6)** PAGES.

Q1 (a) Verilog is a popular Hardware Description Language (HDL) used when working with programmable devices.

i. Explain the purpose of the language and how it interacts to an actual programmable chip.

(4 marks)

ii. Specify **TWO (2)** synthesizable constructs and **TWO (2)** non-synthesizable constructs for Verilog language.

(4 marks)

(b) **Figure Q1(b)i** and **Figure Q1(b)ii** illustrate schematic circuits of 2-to-1 multiplexer and 4-to-1 multiplexer, respectively.

i. Explain the relation between **Figure Q1(b)i** and **Figure Q1(b)ii**.

(4 marks)

ii. Specify the methodology being applied to design the circuit of **Figure Q1(b)ii**.

(1 mark)

iii. Develop a flow chart to specifically illustrate the process to test the functionality of Verilog code in **Figure Q1(b)ii** using Computer Aided Design (CAD) tool.

(7 marks)

Q2 (a) Convert the decimal number -120 into signed 8-bit numbers in the following representations:

i. Sign and magnitude

(2 marks)

ii. 1's complement

(1 mark)

iii. 2's complement

(1 marks)

(b) **Figure Q2(b)** illustrates Functional Block Diagram (FBD) of a four-bit adder-subtractor that is designed using full adder modules. Verilog code of the full adder module is given in **Listing Q2(b)**. Input M controls the operation mode of the FBD.

i. Determine the operation mode of the FBD when $M = 0$ and $M = 1$. Justify your answer.

(3 marks)

ii. Determine S and c values, if $M = 0$, $A = 1010_2$, $B = 1100_2$.

(3 marks)

iii. Write the Verilog gate-level hierarchical description for the FBD of **Figure Q2(b)**.

(10 marks)

Q3 (a) Explain the difference between latch and flip-flop.

(2 marks)

(b) **Figure Q3(b)i** shows a simple sequential circuit, while **Figure Q3(b)ii** is input waveform signals to drive the sequential circuit. Sketch output signals for Q_a, Q_b, and Q_c.

(6 marks)

(c) **Figure Q3(c)** gives sample of input and output relation for a sequence detector to detect a pattern of "101". Finite-State Machine (FSM) uses state diagram for representing every possible state behavior for the detector.

i. Discuss the concept of Finite-State Machine, FSM state diagram.

(4 marks)

ii. Derive state diagram for the FSM to capture all possible state behavior given in **Figure Q3(c)**.

(8 marks)

Q4 A digital system is modelled by register transfer level (RTL) code given in **Listing Q4**. The system loads data when $f = 0$, while adding A and B values when $f = 1$.

(a) Derive datapath unit for the digital system given in **Listing Q4**.

(7 marks)

(b) Design FBD control unit (CU) for the digital system.

(6 marks)

(c) Derive RTL control sequence (RTL-CS) table, for the control vector format *sel1*, *LdA*, *LdB*, *f*, and *done*.

(7 marks)

Q5 Given x and y expressions as follows:

$x = e \times (a + b + c)$ (1)

$y = (a + c) \times (c + d)$ (2)

(a) Restructure the expressions by using coarse-level restructuring technique.

(2 marks)

(b) Create data flow graph (DFG) based on restructured expressions in **Q5(a)**. The DFG must comply the following constraints:

- One multiplier and one adder resource allocation.
- Apply 'as late as possible' (ALAP) register allocation.
- As minimum as possible of total number execution cycles.

(8 marks)

(c) Derive the datapath unit (DU) based on the DFG in **Q5(b)**.

(10 marks)

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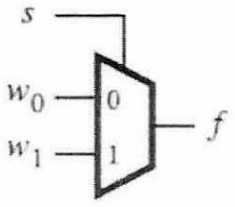

Figure Q1(b)i

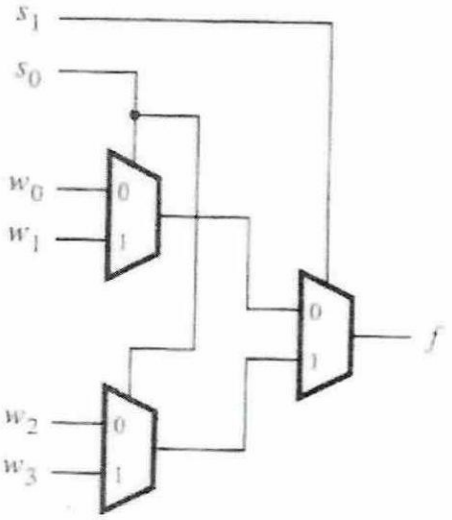

Figure Q1(b)ii

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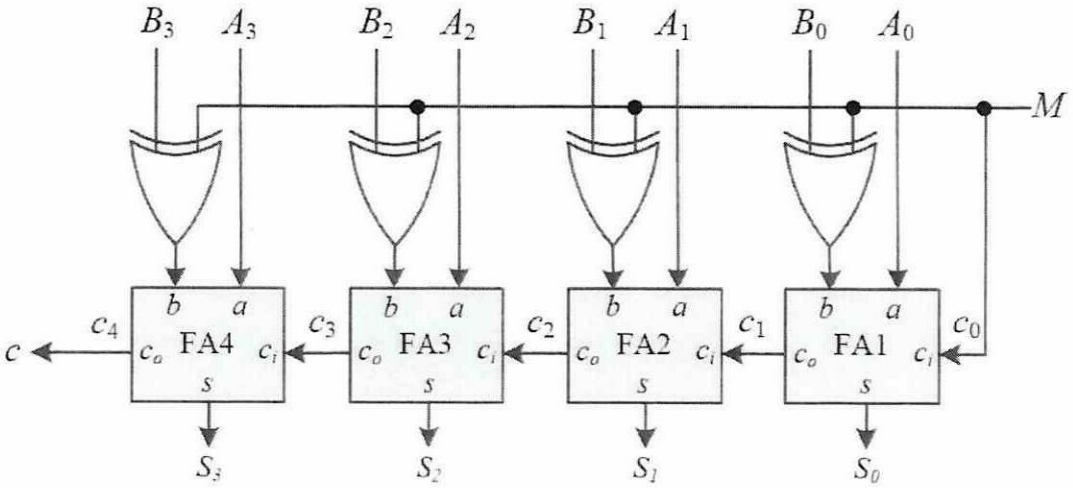

Figure Q2(b)

```
module fulladd (ci, a, b, s, co);
   input ci, a, b;
   output s, co;

   assign s = a^b^ci;
   assign co = (a&b) | (a&ci) | (b&ci);
endmodule
```

Listing Q2(b)

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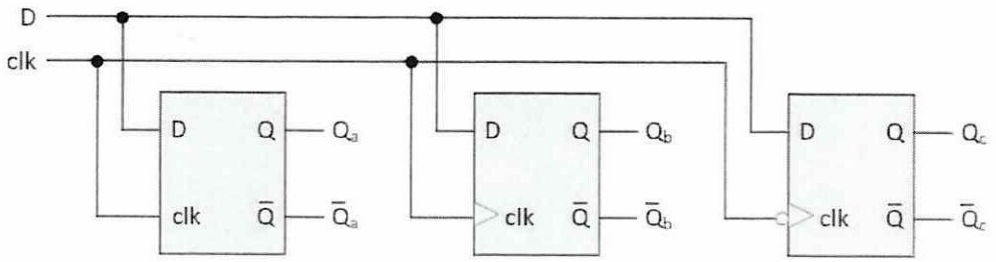

Figure Q3(b)i

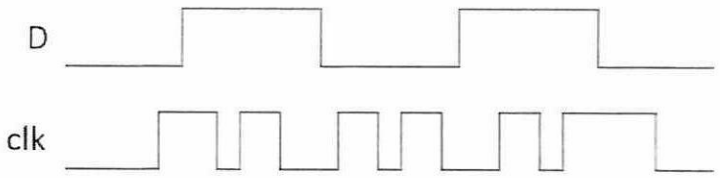

Figure Q3(b)ii

Input, w = 1001010000101010100011101....
Output, Z = 0000010000001010100000001....

Figure Q3(c)

```
S0: Reg1 ← A;
S1: Reg2 ← Reg1;
S2: Reg1 ← B;
S3: Reg1 ← Reg1 + Reg2;
    done
```

Listing Q4