Universiti Tun Hussein Onn Malaysia

UNIVERSITI TUN HUSSEIN ONN MALAYSIA

FINAL EXAMINATION
SEMESTER II
SESSION 2022/2023

COURSE NAME	:	DIGITAL ELECTRONICS
COURSE CODE	:	BEJ 10603 / BEV 10603
PROGRAMME CODE	:	BEJ / BEV
EXAMINATION DATE	:	JULY / AUGUST 2023
DURATION	:	3 HOURS
INSTRUCTION	:	1. ANSWER ALL QUESTIONS 2.THIS FINAL EXAMINATION IS CONDUCTED VIA **CLOSED BOOK.** 3.STUDENTS ARE **PROHIBITED** TO CONSULT THEIR OWN MATERIAL OR ANY EXTERNAL RESOURCES DURING THE EXAMINATION CONDUCTED VIA CLOSED BOOK

THIS QUESTION PAPER CONSISTS OF **EIGHT (8)** PAGES

Q1 (a) A water ride theme park company wants to design an embedded safety system that can shut down the engine if the user falls off the seat during running.

There are THREE independent sensors input labeled as X, Y and Z to produce THREE output signals of M, N and P. Sensor M was embedded in the seat, and sensor N was assigned to the leg support area. While sensor P was assigned to hold the safety key that was attached all the time to the user's wrist. All sensors produce HIGH when pressed or tugged in.

Output M will be HIGH when both inputs X and Y are HIGH.
Output N will be HIGH when both input Z and output M are HIGH.
Output P will be HIGH when both output M is LOW but output Z is HIGH.

(i) Construct the truth table for this system.

(8 marks)

(ii) Analyze the minimized logic equations for outputs X, Y and Z. Simplify the expression by using both the Karnaugh map and Boolean expressions.

(6 marks)

(iii) According to the simplified expressions in **Q1(a)(ii)**, draw the combinational circuit response.

(3 marks)

(b) Given a Boolean expression, $\boldsymbol{m = (A + \overline{B}).(C).(A + B + \overline{C})}$;

(i) Simplify the expression.

(5 marks)

(ii) Analyze the simplified equivalent expression m and draw the circuit using the NOR gate only.

(3 marks)

Q2 (a) Analyze the outputs of the 4-bit comparator (74LS85) as shown in **Figure Q2(a)** using inputs of A0, A1, A2, A3, B0, B1, B2 and B3. All outputs are active-HIGH.

(9 marks)

(b) A full adder system has to be implemented using IC 74LS138 (3 to 8 decoder) as shown in **Figure Q2(b)**.

The output sum, S, and carry, C has an equation of:

$$\text{Sum (A1, A2, A3)} = \prod (0, 1, 2, 4)$$
$$\text{Carry (A1, A2, A3)} = \prod (0, 3, 5, 6)$$

(i) Construct the truth table based on the equation.

(4 marks)

(ii) Analyze the outputs S and C, from **question Q2(b)(i)** in the term product of sum (POS).

(8 marks)

(iii) Implement the obtain POS expression into 3-to-8 decoder as given in **Figure Q2(b)** to function as a full adder system.

(4 marks)

Q3 (a) (i) Describe the difference between latches and flip-flops in terms of their function.

(4 marks)

(ii) List **TWO (2)** types of latches and flip-flops.

(4 marks)

(b) The waveforms of **Figure Q3(b)(ii)** are connected to the circuit of **Figure Q3(b)(i)**. Sketch the S, C and Q waveforms by assuming that Q = 0 initially.

(9 marks)

(c) **Figure Q3(c)(i)** shows a flip-flop circuit. Complete the timing diagram for signals Y and Q in **Figure Q3(c)(ii)**. Assume that Q is at a high level initially.

(8 marks)

Q4 (a) Based on an asynchronous MOD-9 up counter;

(i) Calculate the frequency of the signal at MSB of the counter if a clock frequency of 1.8kHz is applied to the counter.

(2 marks)

(ii) Implement the circuit using IC 74LS93 (4-bit binary counter) as shown in **Figure Q4(a).**

(3 marks)

(b) **Figure Q4(b)** shows the pin assignment for two units of IC 74LS293 (4-bit asynchronous counter). Design a frequency divider circuit using the ICs to produce a 1kHz output from a 50 kHz input.

(5 marks)

(c) **Figure Q4(c)** shows the state transition diagram of a state machine.

(i) Build the excitation table for this state machine.

(5 marks)

(ii) Find the simplest Boolean expression for the circuit using Karnaugh map.

(6 marks)

(iii) Implement the circuit diagram.

(4 marks)

- END OF QUESTIONS –

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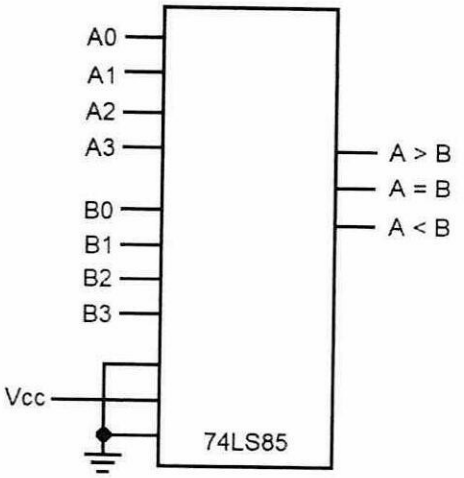

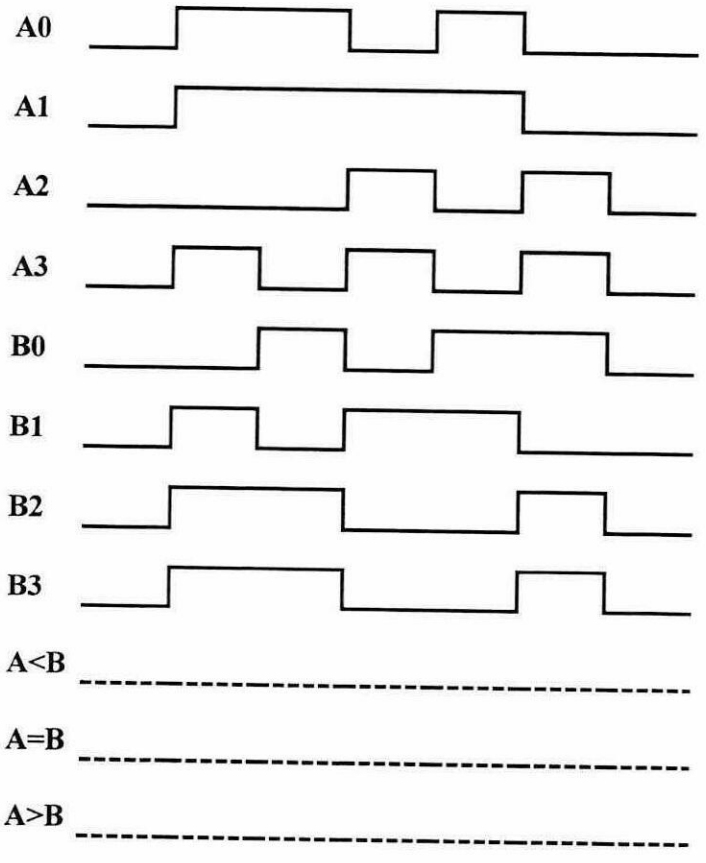

Figure Q2(a)

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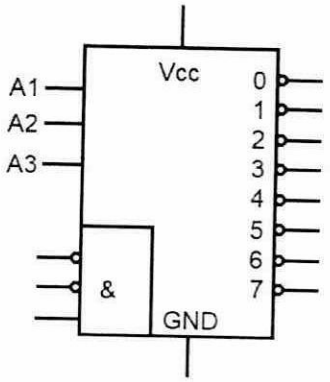

Figure Q2(b)

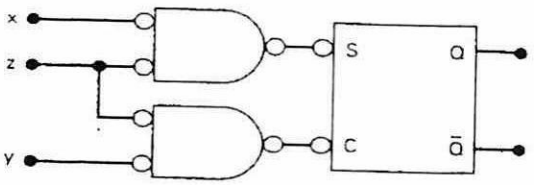

Figure Q3(b)(ii)

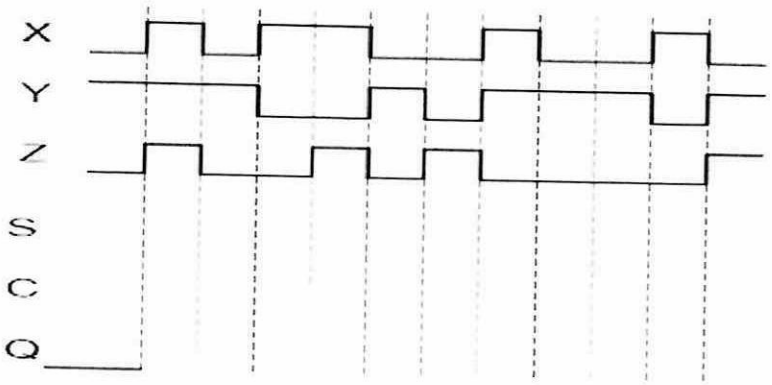

Figure Q3(b)(ii)

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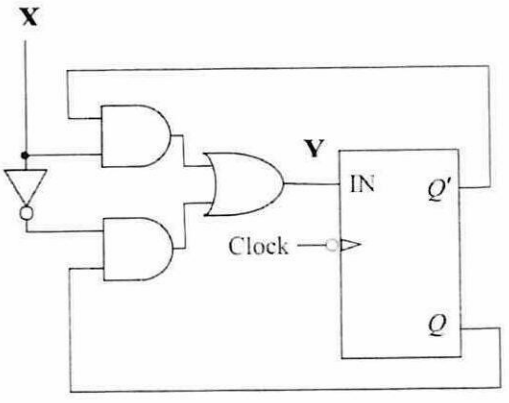

Figure Q3(c)(i)

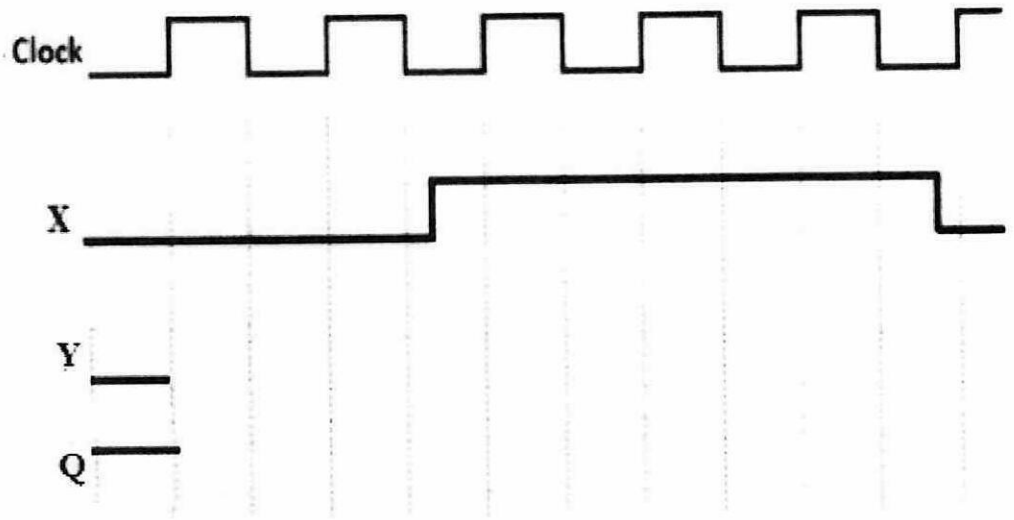

Figure Q3(c)(ii)

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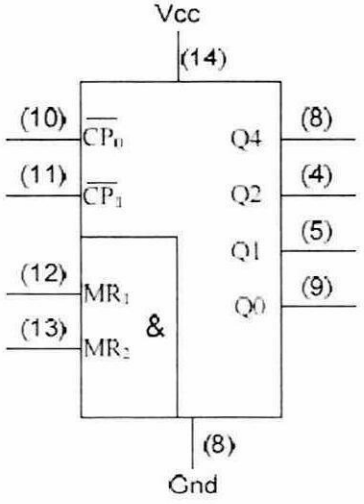
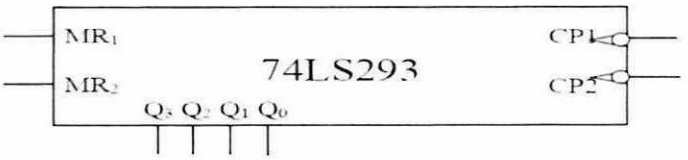


Figure Q4(a)

74LS293 (4-bit Asynchronous Counter)



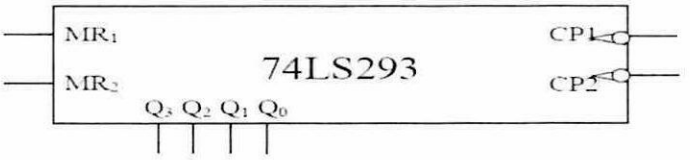


Figure Q4(b)

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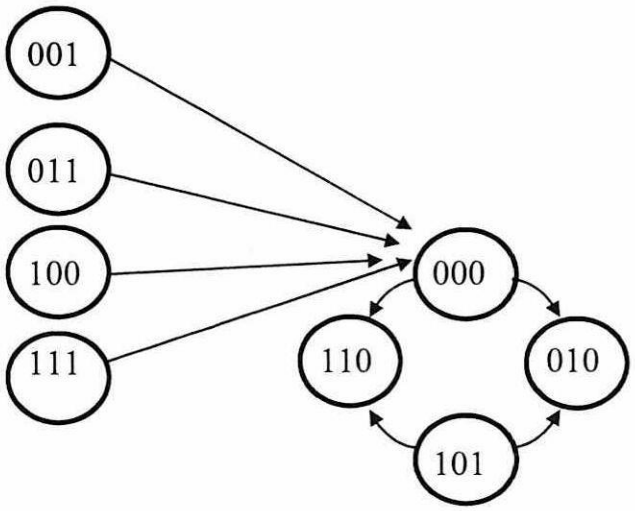

Figure Q4(c)