Universiti Tun Hussein Onn Malaysia

UNIVERSITI TUN HUSSEIN ONN MALAYSIA

FINAL EXAMINATION
SEMESTER II
SESSION 2022/2023

COURSE NAME	:	VLSI SYSTEM
COURSE CODE	:	BEJ 43103
PROGRAMME CODE	:	BEJ
EXAMINATION DATE	:	JULY/ AUGUST 2023
DURATION	:	3 HOURS
INSTRUCTION	:	1. ANSWER ALL QUESTIONS 2.THIS FINAL EXAMINATION IS CONDUCTED VIA **CLOSED BOOK.** 3.STUDENTS ARE **PROHIBITED** TO CONSULT THEIR OWN MATERIAL OR ANY EXTERNAL RESOURCES DURING THE EXAMINATION CONDUCTED VIA CLOSED BOOK

THIS QUESTION PAPER CONSISTS OF **FIVE (5)** PAGES

Q1 (a) Explain in detail **TWO (2)** regions of operation of MOS transistor.

(4 marks)

(b) A digital output is given by the following expression:

$$Y = \overline{(AB + C)(A + D)}$$

(i) Design a fully complementary static CMOS circuit using minimum number of transistors to realize the logic function.

(8 marks)

(ii) Draw the consistent Euler path for the circuit.

(5 marks)

(iii) Draw the most compact stick diagram representing the circuit given by the equation. Clearly label the stick diagram.

(8 marks)

Q2 Given a CMOS circuit in **Figure Q2**.

(a) Analyze the CMOS logic circuit and determine the Boolean expression for output X.

(4 marks)

(b) Determine the size of each transistor to be used in the design such that the circuit will have an equivalent driving capability on an inverter. Given that the minimum transistor length (L) is 2λ and the width (W) is 3λ; and the mobility of the electron is 2 times of the hole's mobility.

(12 marks)

(c) Calculate the total driving strength for inverter and minimal parasitic delay for the circuit.

(4 marks)

(d) Logical Effort (g) is usually used in calculating the delay in VLSI circuits.

(i) State the definition of Logical Effort.

(2 marks)

(ii) Calculate the Logical Effort, g for input A, C and F of the circuit.

(3 marks)

Q3 (a) A block diagram of 8-to-3 (octal-to-binary) encoder is shown in **Figure Q3(a)**.

(i) Formulate the equations for the outputs by tabulating the truth table of the encoder.

(6 marks)

(ii) Build the circuit at transistor level for the outputs, D_2, D_1 and D_0 by using a family logic that can reduce a parasitic capacitance method with a minimum number of transistors.

(6 marks)

(b) **Figure Q3(b)** shows the symbol of 4-to-1 multiplexer used when one of the four data sources selected for a digital process.

(i) Establish the truth table for the multiplexer and obtain the equation for the output Y.

(4 marks)

(ii) Design at transistor level using minimum number of transistors the circuit for output Y using transmission gate method.

(5 marks)

(iii) Modify the multiplexer circuit by employing a pass transistor logic method.

(4 marks)

Q4 (a) **Figure Q4(a)** shows the level sensitive latch circuit.

(i) Examine and describe the operation of the circuit.

(4 marks)

(ii) Determine the type of the latch and obtain the equation for the output of the circuit, Q.

(6 marks)

(b) Generate a complete test set that comprises a minimum number of tests by using path sensitization in the circuit in **Figure Q4(b)**.

(15 marks)

- END OF QUESTIONS –

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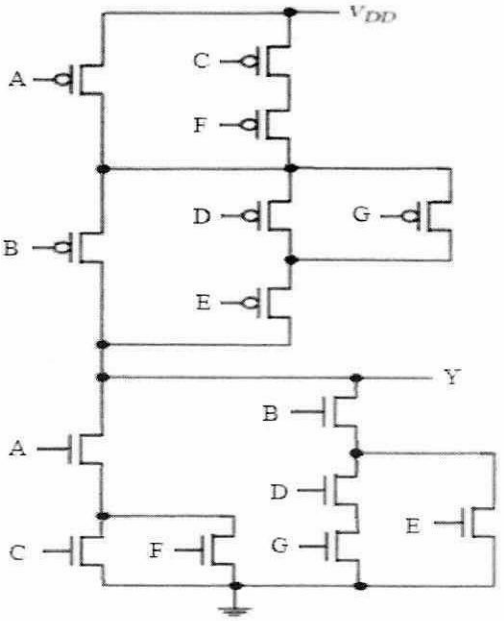

Figure Q2

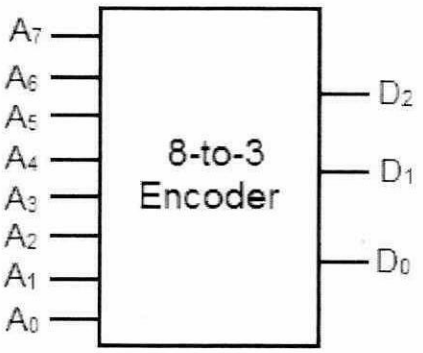

Figure Q3(a)

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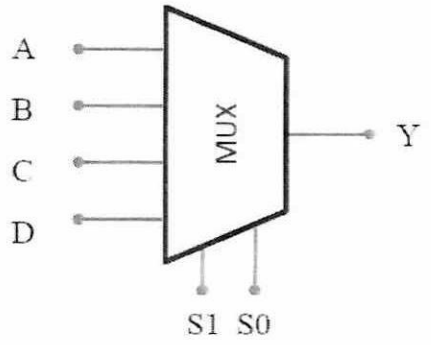

Figure Q3(b)

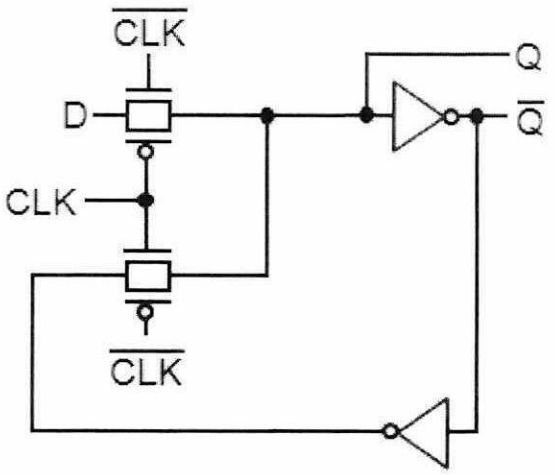

Figure Q4(a)

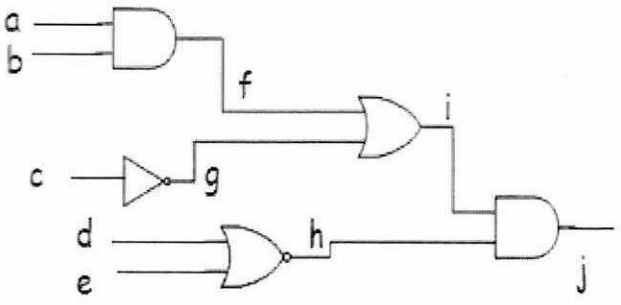

Figure Q4(b)