Universiti Tun Hussein Onn Malaysia

UNIVERSITI TUN HUSSEIN ONN MALAYSIA

FINAL EXAMINATION
SEMESTER II
SESSION 2022/2023

COURSE NAME	:	DIGITAL ELECTRONICS / DIGITAL DEVICES AND CIRCUITS
COURSE CODE	:	BNR 25403 / BNR 23103
PROGRAMME CODE	:	BND / BNE / BNF
EXAMINATION DATE	:	JULY / AUGUST 2023
DURATION	:	3 HOURS
INSTRUCTION	:	1. ANSWER **ALL** QUESTIONS 2. THIS FINAL EXAMINATION IS CONDUCTED VIA **CLOSE BOOK** 3. STUDENTS ARE **PROHIBITED** TO CONSULT THEIR OWN MATERIAL OR ANY EXTERNAL RESOURCES DURING THE EXAMINATION CONDUCTED VIA CLOSED BOOK

THIS QUESTION PAPER CONSISTS OF **THIRTEEN (13)** PAGES

Q1 (a) Determine how many bits are required to represent the following numbers?

(i) 8_{10}

(1 mark)

(ii) 250_8

(1 mark)

(iii) $D631_{16}$

(1 mark)

(b) Perform the following arithmetic operations with signed numbers. Show your calculation steps.

(i) 01001000 + 11000001

(1 marks)

(ii) 11000110 - 00011000

(2 marks)

(iii) Multiply 11001010 (multiplicand) and 01001111 (multiplier)

(2 marks)

(iv) Divide 00111100 by 00010001

(2 marks)

(c) (i) A combination of inverters is shown in **Figure Q1(c)(i)**. If a HIGH input is applied to point A, determine the output at points E and F.

(2 marks)

(ii) If the waveform in **Figure Q1(c)(ii)** is applied to point A in **Figure Q1(c)(i)**, determine the waveforms at points B through F.

(3 marks)

(d) For the following Boolean expression:

$$F(A,B,C,D) = \overline{(A\bar{B} + CD)} + \overline{(\bar{A}\bar{B}CD)}\,\overline{(A\bar{B}C\bar{D})}\,\overline{(\bar{A}CD)}\,\overline{(\bar{B}\bar{D})} + \overline{\overline{ABCD}}$$

(i) Simplify it using DeMorgan's Theorem.

(3 marks)

(ii) From **Q1(d)(i)**, simplify it using Boolean algebra.

(3 marks)

(iii) From **Q1(d)(i)**, produce the truth table and simplify it using Karnaugh Map (KMap). Verify the final answer with the expression obtained in **Q1(d)(ii).**

(4 marks)

Q2 (a) Consider the Boolean function:

$$F(A,B,C,D) = \sum(0,1,3,4,9,11,12,13,14,15)$$

(i) Produce the truth table of the Boolean function.

(2 marks)

(ii) Write the standard SOP expression.

(2 marks)

(iii) Minimize the expression obtained in **Q2(a)(ii)** using KMap and prove it using Boolean theorem.

(6 marks)

(b) Consider the Boolean function:

$$F(A,B,C,D) = \prod(3,4,5,7,13)$$

(i) Produce the truth table and obtain the minimum POS expression by using KMap for the function F(A,B,C,D).

(4 marks)

(ii) If the minimum POS expression for the above function F(A,B,C,D) is

$$F(A,B,C,D) = (\bar{B} + C)(\bar{B} + \bar{D})(A + \bar{D})$$

Identify the possible don't cares that may have existed in the KMap. Show that the minimum POS expression can be obtained by considering the don't cares in the Kmap.

(3 marks)

(iii) Implement the minimum POS expression from **Q2(b)(ii)** in NAND-NAND form.

(3 marks)

(c) Show how the following expressions can be implemented using specified gates:

(i) $X = \overline{AB} + \overline{CD}$ using NAND gates only.

(2 marks)

(ii) $X = AB[C(\overline{DE} + \overline{AB}) + \overline{BCE}]$ using NOR gates only.

(3 marks)

Q3 (a) Circuit in **Figure Q3(a)** has three inputs (A, B and C) and one output (Z). Construct the truth table. Refer to **APPENDIX A** to know the pin assignment of SN7400N and SN7432N.

(10 marks)

(b) **Figure Q3(b)** shows a multiplexer 74LS151 (8 line-to-1 line multiplexer). Based on the truth table obtained in part **Q3(a)**, implement the circuit of function Z using 74LS151 multiplexer. Show all connections and please answer in **APPENDIX B**.

(6 marks)

(c) Implement the following Boolean expression using IC 74LS138 (3-to-8 decoder) in **Figure Q3(c)**. Symbol for IC 74LS138 is shown in **APPENDIX C** for the internal circuitry and pins assignment of 74LS138 (3-to-8 decoder). Show all connections and please answer in **APPENDIX C.**

$$Z = \overline{(\overline{A}B + B + \overline{C} + AB)}$$

(9 marks)

Q4 (a) What are the differences between latch and flip-flop?

(2 marks)

(b) Given the flip-flop in **Figure Q4(b)(i)**, complete the timing diagram for Q of **Figure Q4(b)(ii)**. Assume that Q is at high level initially. Please answer in **APPENDIX D**.

(4 marks)

(c) A binary counter is a state machine that is made from a series of flip-flops. Design a counter that able to produce the following binary sequence.

1, 4, 3, 7, 6, 2, 1.....

(15 marks)

(d) An analogy for a shift register is a conveyor belt as shown in **Figure Q4(d)**. The illustration shows a single conveyor belt at four different times. State and explain which shift register operations of the following sequence represents.

(4 marks)

- END OF QUESTIONS -

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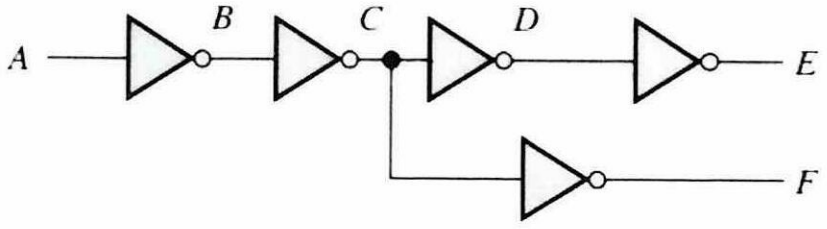

Figure Q1(c)(i)

Figure Q1(c)(ii)

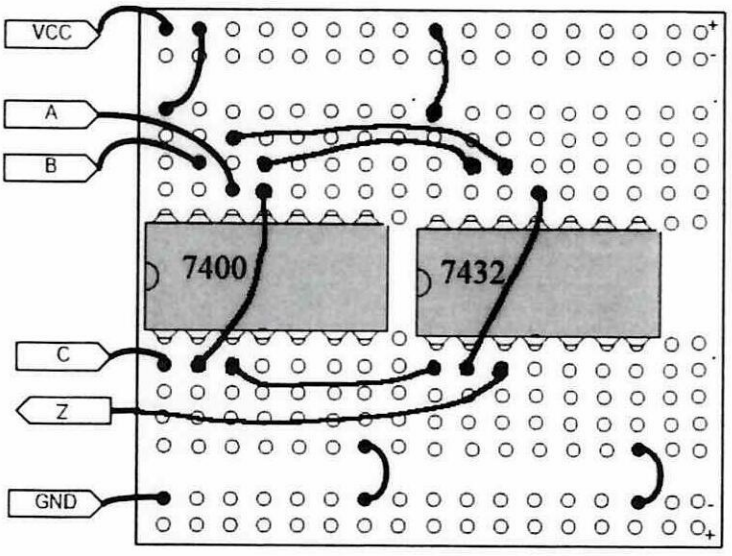

Figure Q3(a)

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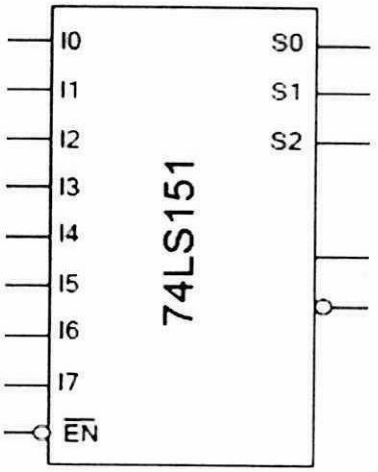

Figure Q3(b)

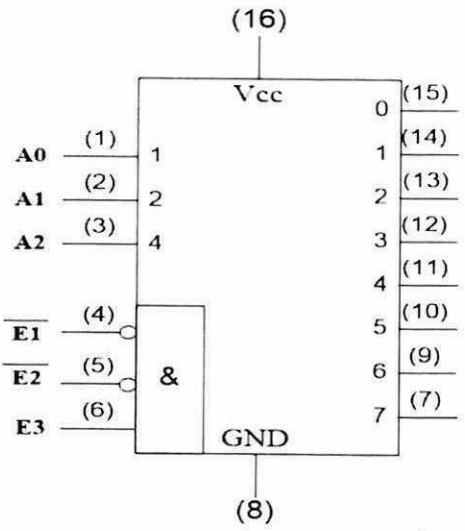

Figure Q3(c)

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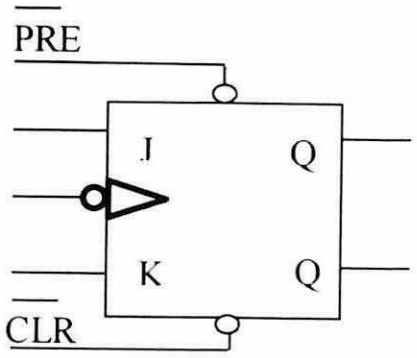

Figure Q4(b)(i)

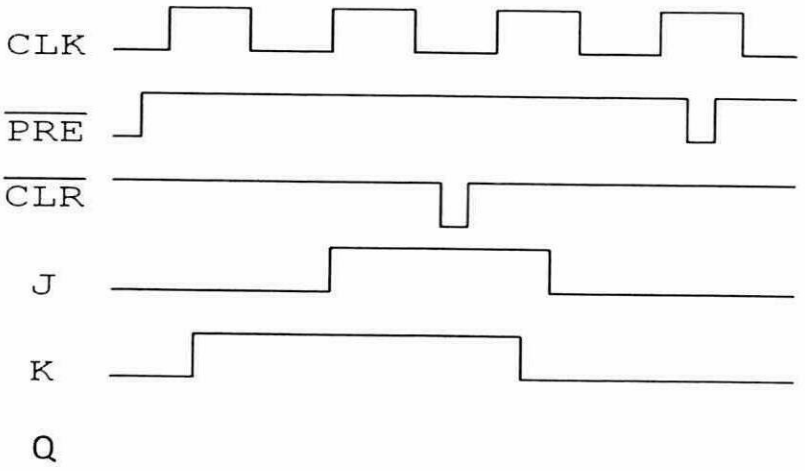

Figure Q4(b)(ii)

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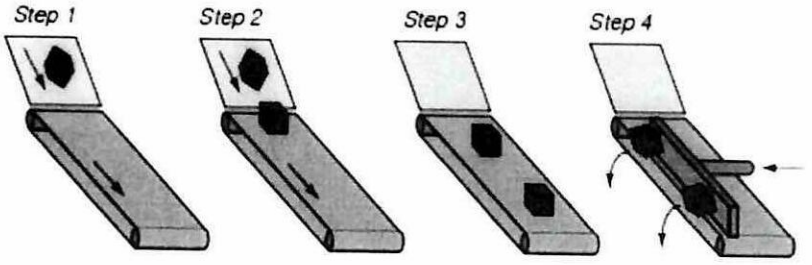
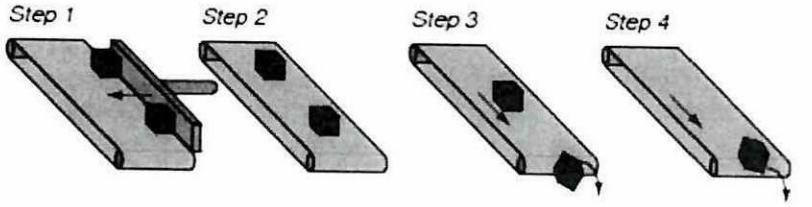


(i)



(ii)

Figure Q4(d)

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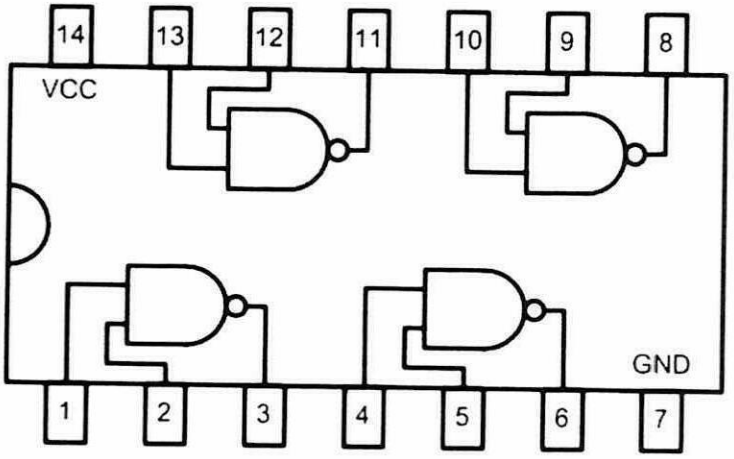
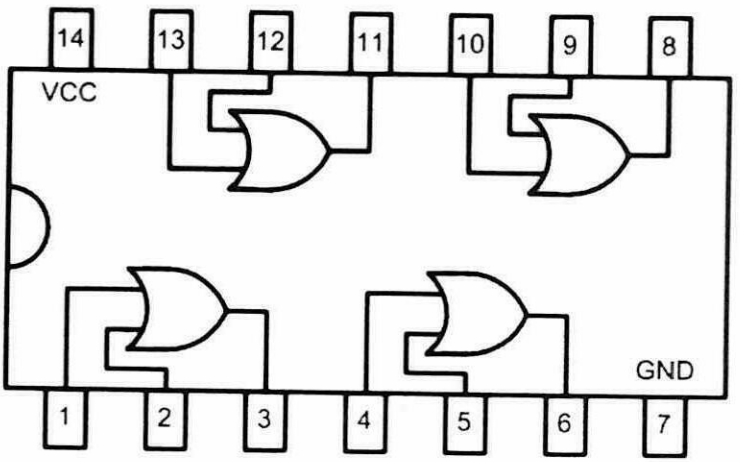
APPENDIX A

PIN ASSIGNMENT AND INTERNAL CIRCUITRY



7400 Quad 2 Input NAND



7432 Quad 2 Input OR

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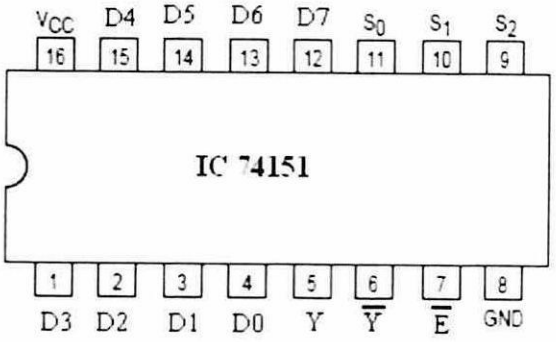
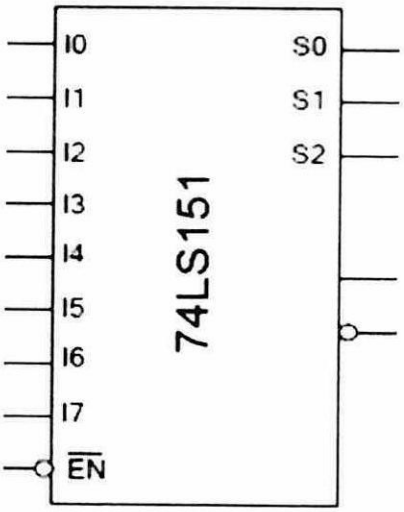
APPENDIX B

PIN ASSIGNMENT AND INTERNAL CIRCUITRY

74LS151 (8 line-to-1 line Multiplexer)





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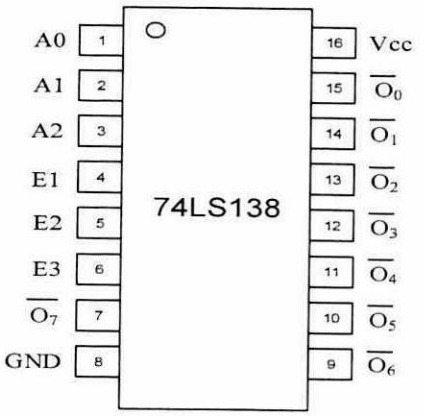
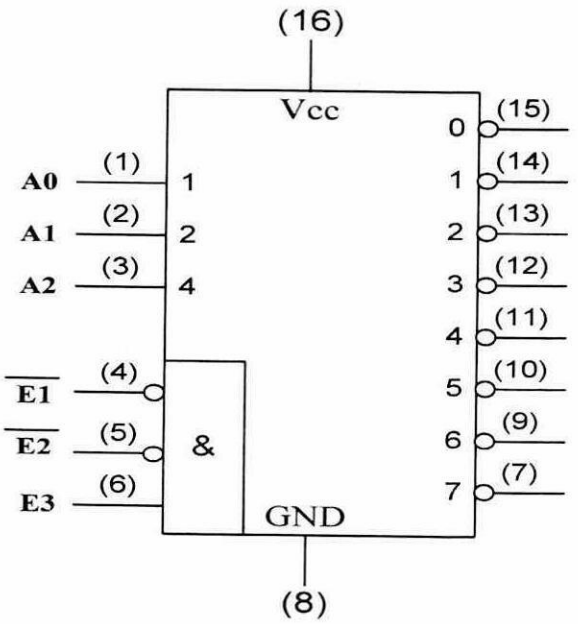
APPENDIX C

PIN ASSIGNMENT AND INTERNAL CIRCUITRY

74LS138 (3-to-8 Decoder)





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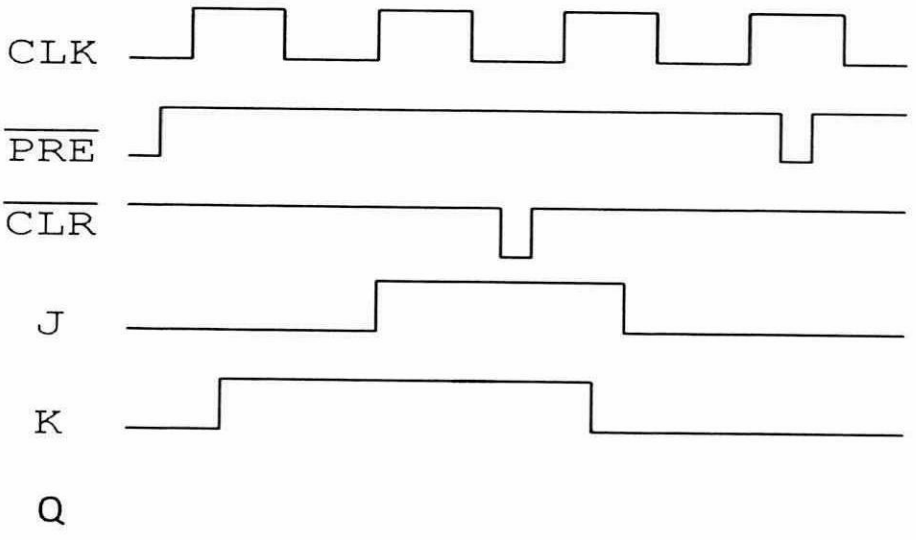
APPENDIX D



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APPENDIX E

Rules of Boolean Algebra

1. $A + 0 = A$	**7.** $A \cdot A = A$
2. $A + 1 = 1$	**8.** $A \cdot \overline{A} = 0$
3. $A \cdot 0 = 0$	**9.** $\overline{\overline{A}} = A$
4. $A \cdot 1 = A$	**10.** $A + AB = A$
5. $A + A = A$	**11.** $A + \overline{A}B = A + B$
6. $A + \overline{A} = 1$	**12.** $(A + B)(A + C) = A + BC$

A, *B*, or *C* can represent a single variable or a combination of variables.