Universiti Tun Hussein Onn Malaysia

UNIVERSITI TUN HUSSEIN ONN MALAYSIA

FINAL EXAMINATION
SEMESTER II
SESSION 2023/2024

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COURSE CODE	:	DAE 21203
PROGRAMME CODE	:	DAE
EXAMINATION DATE	:	JULY 2024
DURATION	:	2 HOURS 30 MINUTES
INSTRUCTION	:	1. ANSWER **ALL** QUESTIONS 2. THIS FINAL EXAMINATION IS CONDUCTED VIA ☐ Open book ☒ Closed book 3. STUDENTS ARE **PROHIBITED** TO CONSULT THEIR OWN MATERIAL OR ANY EXTERNAL RESOURCES DURING THE EXAMINATION CONDUCTED VIA CLOSED BOOK

THIS QUESTION PAPER CONSISTS OF **EIGHTEEN (18)** PAGES

PART A: ANSWER ALL QUESTIONS IN THE OMR FORM (40 MARKS)

Q1 According to De Morgan theorems, the following equality(s) is (are) correct

A. $\overline{PQ} = \overline{P} + \overline{Q}$
B. $\overline{A + B + C} = \overline{A}\,\overline{B}\,\overline{C}$
C. $\overline{XYZ} = \overline{X} + \overline{Y} + \overline{Z}$
D. All of these

Q2 The two digits hexadecimal number which has largest value is ___ which corresponds to _____

A. FE, 255 decimal
B. FF, 254 decimal
C. FF, 255 decimal
D. EF, 245 decimal

Q3 Which one of the following logical operations is performed by the digital circuit shown in **Figure Q3**?

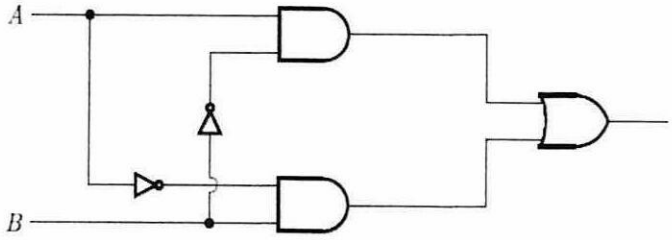


Figure Q3

A. NOR
B. XOR
C. NAND
D. OR

Q4 The most suitable gate to check whether the parity number of 1s in a digital word is even or odd is _____

A. XOR
B. NOR
C. NAND
D. AND, OR and NOT

Q5 The truth table of a circuit is shown in **Figure Q5**. The expression for $\bar{X}$ is equal to

A	B	C	X
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0

Figure Q5

A. $AB + \bar{B}C + B\bar{C}$
B. $\bar{B}C$
C. $\bar{B}C + AB\bar{C}$
D. $AB\bar{C}$

Q6 In the circuit of **Figure Q6**, the output Z is

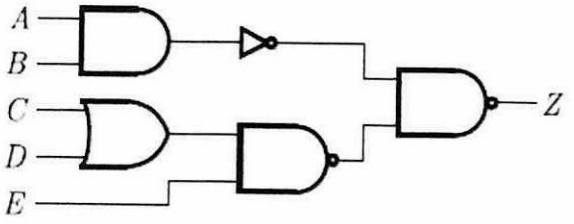


Figure Q6

A. $AB + (C + D)E$
B. $AB + CD + E$
C. $AB(C + D)E$
D. $AB + CDE$

Q7 The switching circuit in the **Figure Q7** can be expressed in binary logic notation as

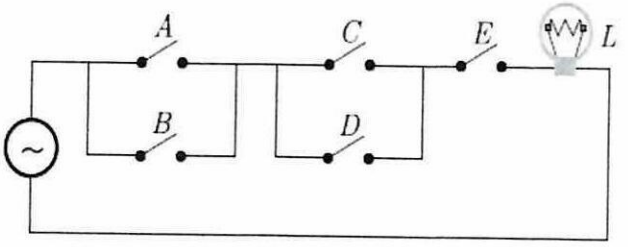


Figure Q7

A. $L = (A + B)(C + D)E$
B. $L = AB + CD + E$
C. $L = E + (A + B)(C + D)$
D. $L = (AB + CD)E$

Q8 What is the hold condition of a flip-flop?

A. both S and R inputs activated
B. no active S or R input
C. only S is active
D. only R is active

Q9 How can parallel data be taken out of a shift register simultaneously?

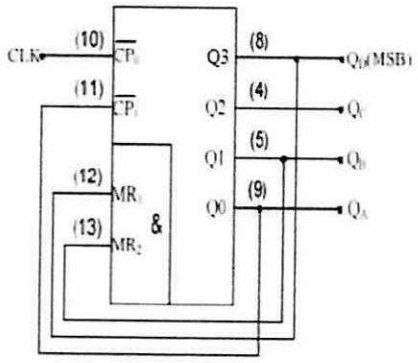
A. Use the Q output of the first FF.
B. Use the Q output of the last FF.
C. Tie all the Q outputs together.
D. Use the Q output of each FF.

Q10 In what type of shift register do we have access to only the leftmost and rightmost flip-flops?

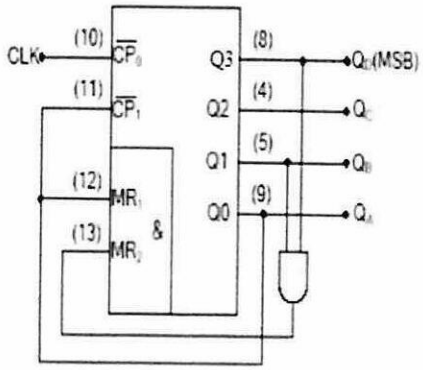
A. Serial-in serial-out shift register
B. Parallel-in serial-out shift register
C. Parallel-in parallel-out shift register
D. Serial-in parallel-out shift register

Q11 Which of the following shows the connection for MOD-6 counter using a decade counter?

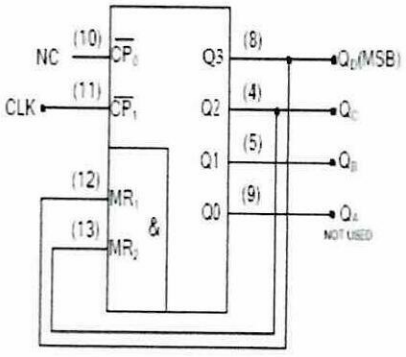
A.



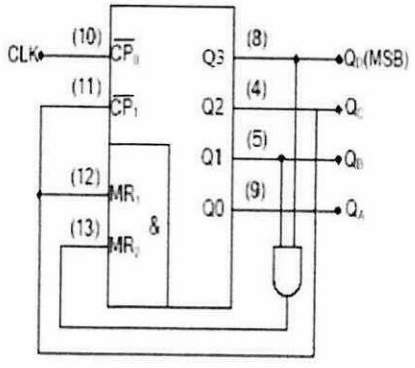
C.



B.



D.



Q12 What is the difference between a LATCH and a FLIP-FLOP?

A. Latch is a level sensitive device while flip-flop is an edge sensitive device.

B. Latches take less gates (also less power) to implement than flip-flops.

C. Latch is sensitive to glitches on enable pin, whereas flip-flop is immune to glitches.

D. All above

Q13 To expand a 4-bit parallel adder to an 8-bit parallel adder you must

A. use 4-bit adders with no connections.

B. use eight 4-bit adders with no interconnections.

C. use two 4-bit adders and connect to the sum outputs of one to the bit output of the other.

D. use two 4-bit adders with the carry output of one connected to the carry input of the other.

Q14 Which of the following input and output value are **incorrect** for the 4-bit parallel binary adder/subtractor circuit in **Figure Q14**?

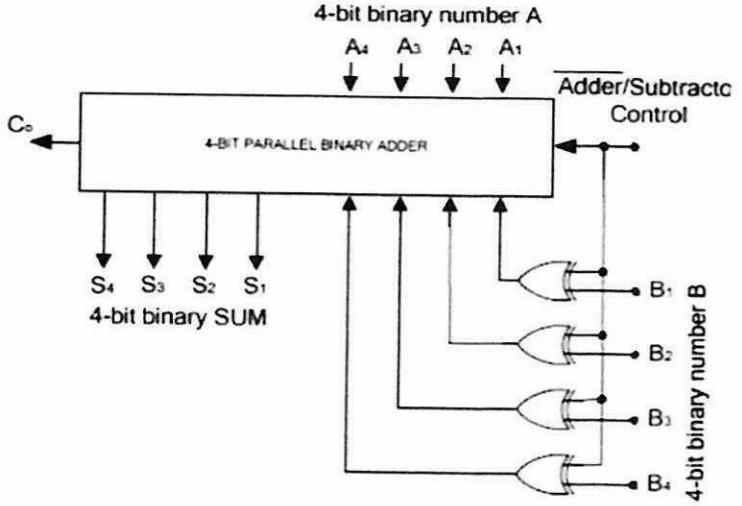


Figure Q14

	[A]	[B]	$\overline{\text{Adder/Subtractor}}$	Cout	[Σ]
A.	1101	0110	0	1	0011
B.	1001	1000	0	1	0001
C.	1111	1011	1	1	0100
D.	0101	1000	1	0	1011

Q15 Data selectors are basically the same as

A. decoders
B. demultiplexers
C. multiplexers
D. encoders

Q16 What is the device shown in **Figure Q16?**

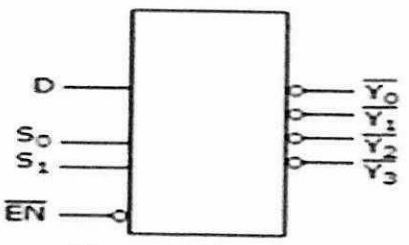


Figure Q16

A. Comparator
B. Multiplexer
C. Inverter
D. Demultiplexer

Q17 In 1-to-8 demultiplexer, how many select lines are required?

A. 2
B. 3
C. 4
D. 5

Q18 If a 74LS85 magnitude comparator has A = 1011 and B = 1001 on the inputs, the outputs are:

A. A>B = 0, A<B = 1, A=B = 0
B. A>B = 1, A<B = 1, A=B = 0
C. A>B = 1, A<B = 0, A=B = 0
D. A>B = 0, A<B = 0, A=B = 1

Q19 The full adder shown by **Figure Q19** is tested under all input conditions with the input waveforms shown. From your observation of the SUM and C_{OUT} waveforms, is it operating properly, and if not, what is the most likely fault?

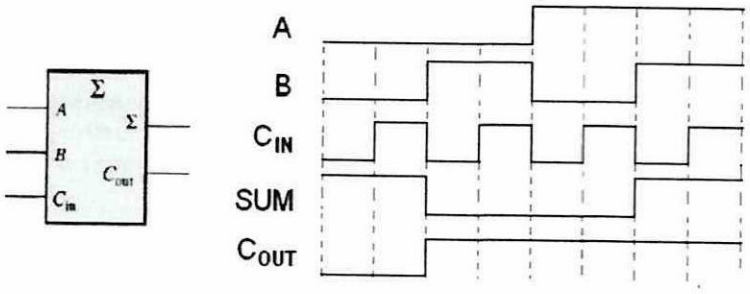


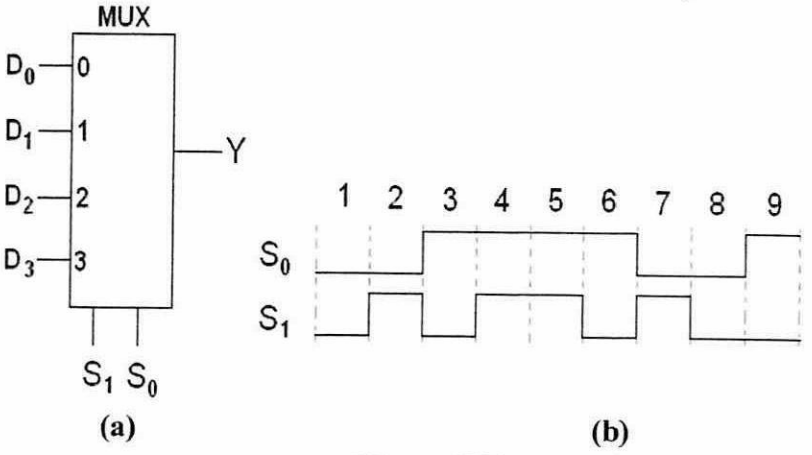
Figure Q19

A. Yes, the output SUM and C_{OUT} are correct.
B. No, the input B is accidentally connected to V_{CC}.
C. No, the input C_{IN} is accidentally connected to V_{CC}.
D. No, the input A is accidentally connected to V_{CC}.

Q20 Table shown is a truth table for a 4-to-2 line priority encoder. Which of the inputs and outputs combination is **correct**?

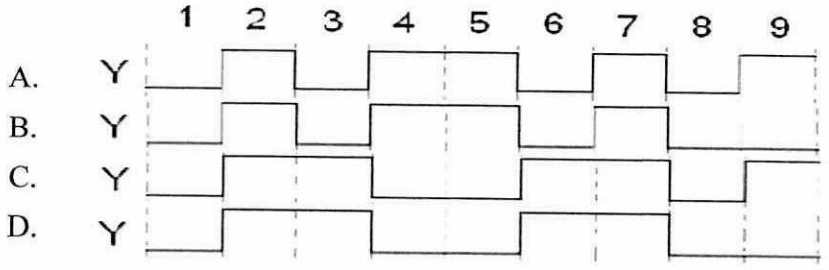
	Inputs					Outputs	
	En	D0	D1	D2	D3	A1	A0
A.	0	0	0	0	1	x	x
B.	1	1	0	0	1	0	0
C.	1	0	1	0	1	0	1
D.	1	0	0	1	1	1	1

Q21 The following data input has been applied to the multiplexer shown in **Figure Q21(a)**: D_0=0, D_1=1, D_2=1, and D_3=0. The data-select inputs to the multiplexer are sequenced as shown by the waveforms in **Figure Q21(b)**, determine the output waveform.



(a) **(b)**

Figure Q21



Q22 What does the combinational logic circuit in **Figure Q22** represent?

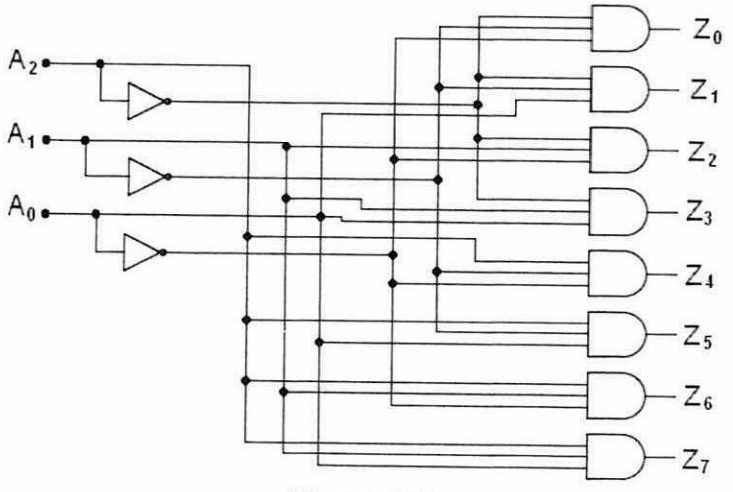


Figure Q22

A. 3-to-8 decoder
B. BCD-to-7 segment decoder
C. 3-to-8 encoder
D. 8-to-3 encoder

Q23 Regarding a D latch, _____.

A. the Q output follows the D input when EN is LOW
B. the Q output is opposite the D input when EN is LOW
C. the Q output follows the D input when EN is HIGH
D. the Q output is HIGH regardless of EN's input state

Q24 A _____ is a combinational circuit element that selects data from one of many inputs and directs it to a single output.

A. encoder
B. decoder
C. multiplexer
D. demultiplexer

Q25 A JK flip-flop is presently in the SET state and must remain SET on the next clock pulse. What is the input J and K?

A. J must be 1 and K must be 1
B. J must be 1 and K must be 0
C. J must be 0 and K must be 0
D. Answer (B) and (C)

Q26 Asynchronous counters are also known as ripple counters. How many JK flip-flops are needed to build MOD-32 counters?

A. 4
B. 5
C. 6
D. 7

Q27 In 1-to-4 multiplexer, if S1 = 1 and S2 = 1, then the output will be

A. *ZO*
B. *Z1*
C. *Z2*
D. *Z3*

Q28 Which of the following quantities is a digital quantity?

A. Altitude of an aircraft
B. Current through a resistor
C. Pressure in a bicycle
D. The amount of time before the buzzer goes off

Q29 Procedures for the design of combinational circuits are:

I. From the word description of the problem, identify the inputs and outputs and draw a block diagram.
II. Draw the truth table such that it completely describes the operation of the circuit for different combinations of inputs.
III. Simplify the switching expression(s) for the output(s).
IV. Implement the simplified expression using logic gates.
V. Write down the switching expression(s) for the output(s).

A. II, III, IV, V, I
B. I, IV, V, II, III
C. I, II, V, III, IV
D. I, II, III, IV, V

Q30 The binary representation of BCD code 00101001_{BCD} is

A. 0011101_2
B. 0110101_2
C. 1101001_2
D. 0101011_2

Q31 1's complement of 1011101 is _____

A. 0101110
B. 1001101
C. 0100010
D. 1100101

Q32 Determine the value of 10111100_2 if it is expressed in 2's complement form.

A. -68_{10}
B. -67_{10}
C. -60_{10}
D. -66_{10}

Q33 On a positive edge-triggered S-R flip-flop, the outputs reflect the input condition when

A. the clock pulse is LOW
B. the clock pulse is HIGH
C. the clock pulse transitions from LOW to HIGH
D. the clock pulse transitions from HIGH to LOW

Q34 An invalid condition in the operation of an active-HIGH input S-R latch occurs when _____.

A. HIGHs are applied simultaneously to both inputs S and R
B. LOWs are applied simultaneously to both inputs S and R
C. a LOW is applied to the S input while a HIGH is applied to the R input
D. a HIGH is applied to the S input while a LOW is applied to the R input

Q35 Consider the given circuit diagram in **Figure Q35** of switching of light from two different switches. The input conditions needed to turn on LED is

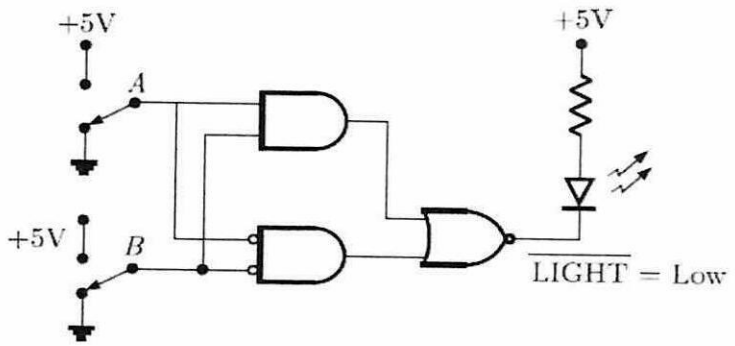


Figure Q35

A. $A = B = 1$
B. $A = 1; B = 0$
C. $A = B = 0$
D. Both (A) and (B)

Q36 The elevator door should open if the elevator is stopped, it is at the same level with the floor, and the timer has not expired, or if the elevator is stopped, it is at the same level with the floor, and a button is pressed.
If D = Elevator door opens; S = Elevator is stopped; F = Same level with the floor; T = Timer expired; B = Button pressed.
Which of the following Boolean expression represents the above condition?

A. $D = SF\bar{T} + SFB$
B. $D = SF + \bar{T}B$
C. $D = SF\bar{T}B$
D. $D = (S + F)\,\bar{T}B$

Q37 A copy machine generates of a stop sign S, to stop the machine operation and energize and indicates light if according to either of the following conditions exists:
(1) There is no paper in the paper feeder tray.
(2) The two micro-switches in the paper path are activated, indicating a jam in the paper path.
The presence of paper in the feeder tray is indicated by a high at logic signal P as shown in **Figure Q37**. Which of the following represents the correct logic circuit to get HIGH output at S?

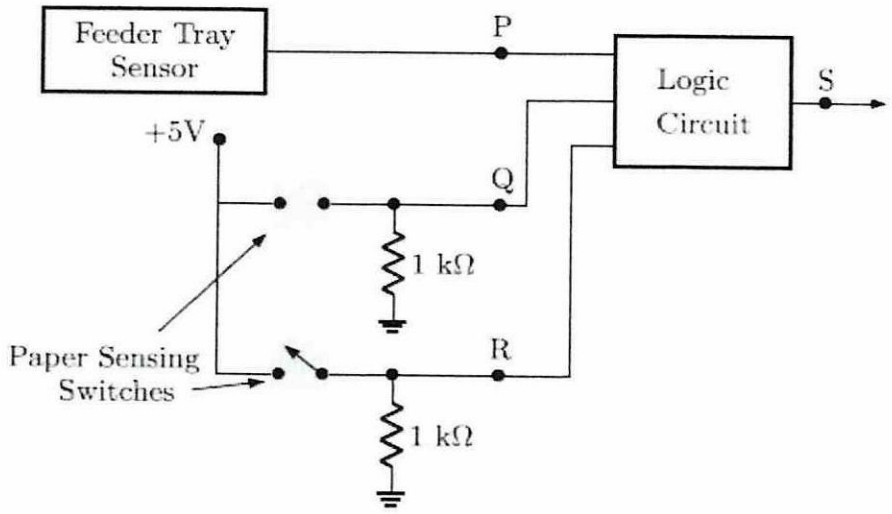
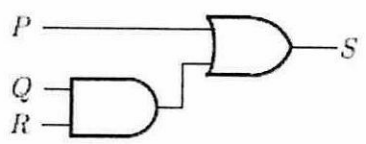
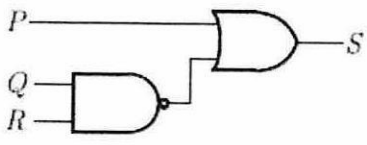
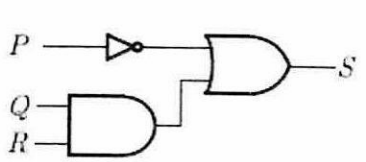
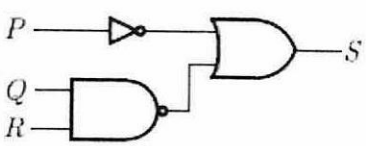


Figure Q37

A.


B.


C.


D.


Q38 The bit sequence 0010 is serially entered (right-most bit first) into a 4-bit parallel out shift register that is initially cleared. What are the Q outputs after two clock pulses?

A. 0000
B. 0010
C. 1000
D. 1111

Q39 In a natural food restaurant, fruit is offered for dessert but only in certain combinations. One choice is either orange or apple or both. Another choice is either mango and apple or neither. A third choice is orange, but if you choose orange, then you must also take banana. If the fruits are represented by their first alphabet of the name, then the logical expression that specifies the fruit available for desert in the simplified form is

A. $A + B$
B. $A + O$
C. $M + O$
D. $M + B$

Q40 Consider the statements below.

1. If the output waveform from an OR gate is the same as the waveform at one of its inputs, the other input is being held permanently LOW.
2. If the output waveform from an OR gate is always HIGH, one of its inputs is being held permanently HIGH.

The statement, which is always true, is;

A. Both 1 and 2
B. Only 1
C. 2
D. None of the above

PART B: ANSWER ALL QUESTIONS IN THE QUESTION BOOKLET (60 MARKS)

Q1 Mr R. Jerry has invested a huge amount of money in the stock market and does not trust just anyone to give him buying and selling information. Before he buys a certain stock, he must get input from three sources. His first source is Pain Webster, a famous stockbroker. His second source is Megan Cash, a self-made millionaire in the stock market, and his third source is Madame LaZora, a world-famous psychic. After several months of receiving advice from all three, he has come to the following conclusions:

- Buy if Pain and Megan both say 'yes' and the psychic says 'no'.
- Buy if the psychic says 'yes'.
- Do not buy otherwise.

(a) Produce a truth table and find the minimized Boolean function to implement the logic telling Mr R. Jerry when to buy stocks.

(6 marks)

ANSWER:

(b) Produce the logic circuit to realize the logic system in Q1(a)

(4 marks)

ANSWER:

(c) Implement the circuit obtained in Q1(b) using two inputs NAND gate only with minimal number of gates.

(4 marks)

ANSWER:

Q2 **Figure Q2.1** shows a shaft encoder disc system with a fixed pattern that measures the angle rotation in rotating machine. The encoder rotates in the anti-clockwise direction. Three light sources are used to shine light through each of three concentric rings on the encoder and are detected by the three photo detectors on the other side of the encoder disc. The most inner ring encodes the least significant bit (LSB) of the angle. In this way, one revolution is divided into 8 separate segments where segment 0 is from 0° to 45°, segment 1 is from 45° to 90°, and so on up to and including segment 7. Light cannot penetrate through the shaded region of the disc. Each photo detector produces logic '1' if light is detected and a logic '0' if otherwise. Produce the truth table showing the segment and the corresponding signals G2, G1 and G0.

(8 marks)

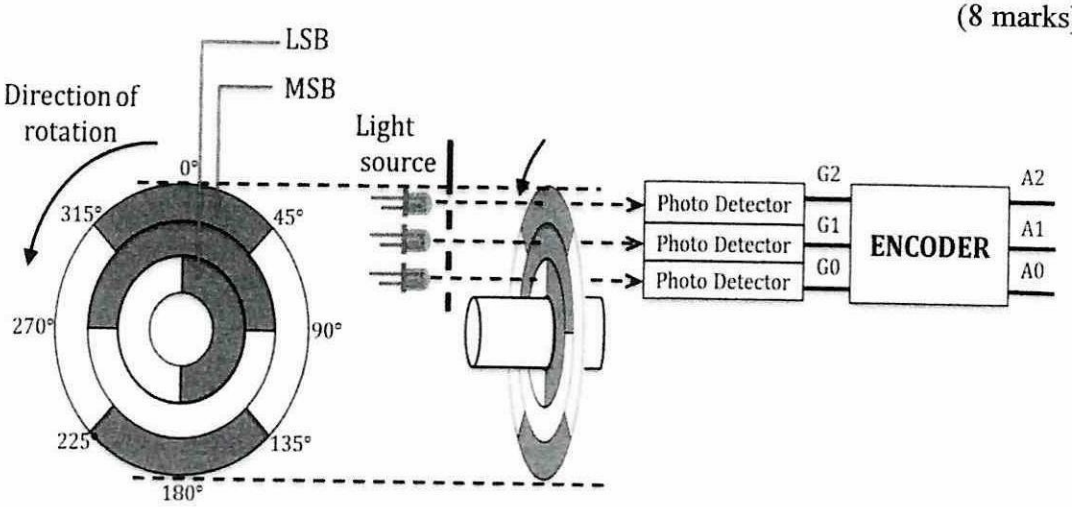
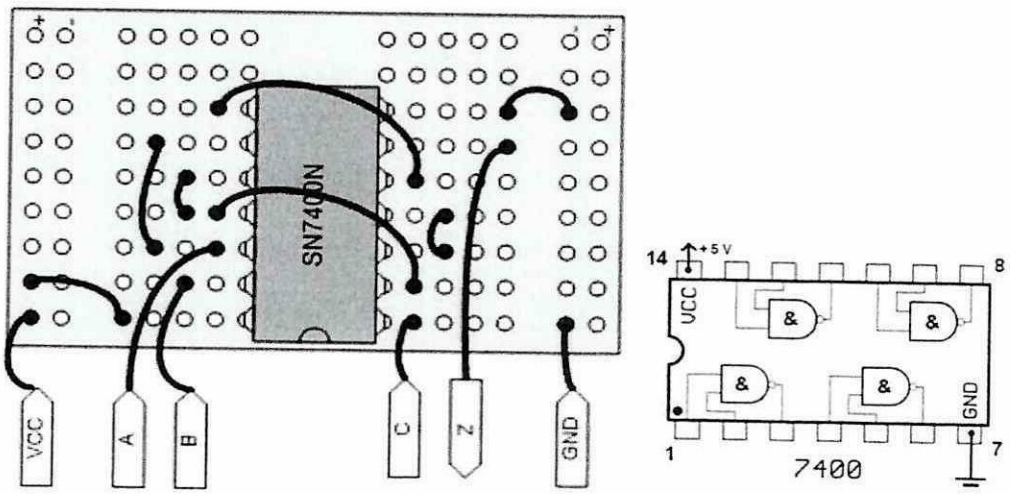


Figure Q2.1

ANSWER:

Q3 (a) Circuit in **Figure Q3(a)(i)** has three inputs (A, B and C) and one output (Z). Produce the truth table. Refer to **Figure Q3(a)(ii)** for pin assignment.

(7 marks)



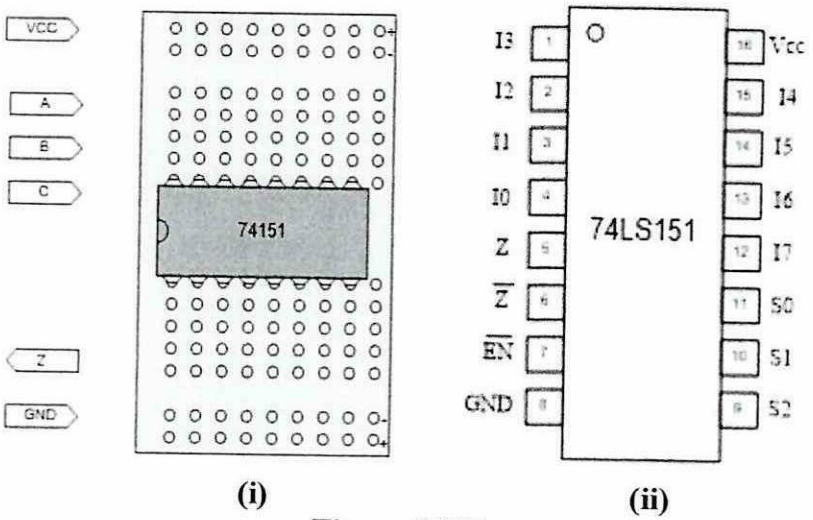
(i) **(ii)**

Figure Q3(a)

ANSWER:

(b) Based on truth table you obtained in **Q3(a)**, implement the circuit using multiplexer in **Figure Q3(b)(i)**. Show all connections. Refer to **Figure Q3(b)(ii)** for pin assignment.

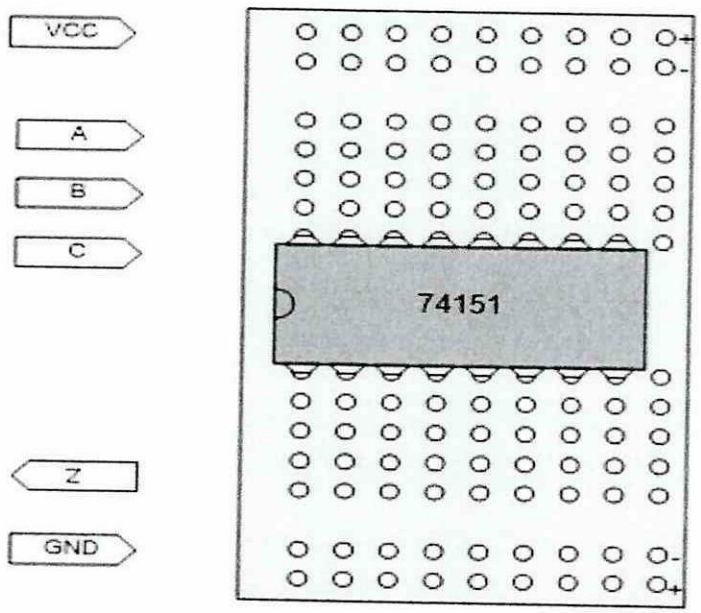
(7 marks)



(i) **(ii)**

Figure Q3(b)

ANSWER:



Q4 (a) Given J, K, $\overline{PRESET}$, $\overline{CLEAR}$ and *NGT-Clk* input waveforms for a JK flip-flop as shown in **Figure Q4(a)**, sketch for output $\overline{Q}$.

(6 marks)

ANSWER:

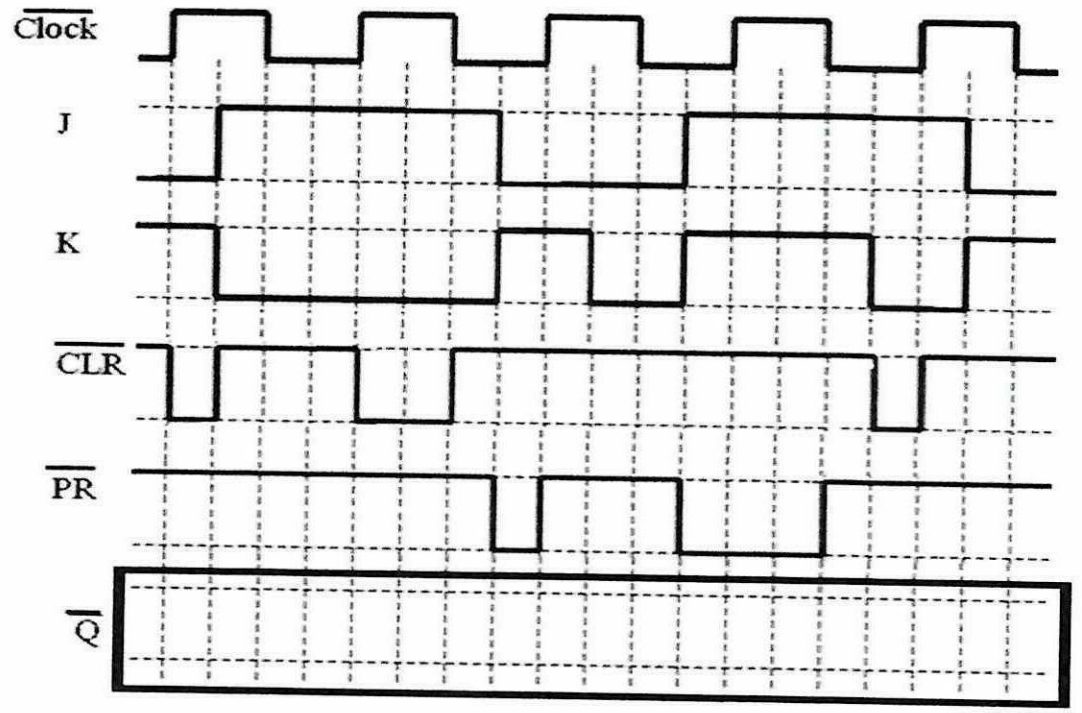


Figure Q4(a)

(b) Design an asynchronous down counter using JK flip-flop counting from 111_2 to 010_2 and label the circuit completely.

(7 marks)

ANSWER:

(c) Obtain the Boolean expression of a synchronous counter using JK flip-flop to count sequence of $11_2 \rightarrow 01_2 \rightarrow 10_2 \rightarrow 00_2$ and repeat. The JK excitation table is shown in **Table Q4(c)**. Show all steps and the design should include the following:

Table Q4(c): JK FF's Excitation Table

Q(t)	Q(t+1)	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

(i) State diagram and excitation table.

(6 marks)

ANSWER:

(ii) K-maps to generate simplified expressions.

(5 marks)

ANSWER:

- END OF QUESTIONS –