Universiti Tun Hussein Onn Malaysia

UNIVERSITI TUN HUSSEIN ONN MALAYSIA

FINAL EXAMINATION
SEMESTER I
SESSION 2017/2018

COURSE NAME	:	LOGIC SYSTEMS
COURSE CODE	:	DAE 21603
PROGRAMME	:	2 DAE
EXAMINATION DATE	:	DECEMBER 2017/ JANUARY 2018
DURATION	:	2 HOURS AND 30 MINUTES
INSTRUCTION	:	SECTION A ANSWER ALL QUESTIONS SECTION B ANSWER **TWO (2)** QUESTIONS ONLY

THIS QUESTION PAPER CONSISTS OF **TEN (10)** PAGES

SECTION A

Q1 (a) Explain **two (2)** primary type of a logic circuit.

(3 marks)

(b) With the aid of diagrams, show the difference between latches and flip-flops.

(3 marks)

(c) With the aid of truth tables, describe the differences between the following flip-flops

(i) RS flip flop.
(ii) JK flip-flop.
(iii) D flip-flop.

(12 marks)

(d) Given J, K, and Clock input for a JK flip-flop in **Figure Q1(d).**

(i) Draw the Q1 output waveform

(4 marks)

(ii) Draw the $\overline{Q2}$ output waveform

(3 marks)

Q2 (a) Design a synchronous counter using JK flip-flop to count 4 digits. The count sequence is 2,0,3,1 and repeat. The JK excitation table is shown in **Table 1**. Show all steps and the design should include the following :

(i) State diagram

(2 marks)

(ii) Circuit excitation table used to determine JK flip-flop inputs.

(5 marks)

(iii) K-maps used to generate minimal expressions for JK inputs.

(5 marks)

(iv) Logic circuit.

(3 marks)

(b) Explain **four (4)** mode of data movement in shift register.

(4 marks)

(c) (i) Determine the number of flip-flops needed to construct a shift register capable of storing a 5-bit binary number.

(1 marks)

(ii) Draw the logic diagram as a serial input/output shift register.

(5 marks)

SECTION B

Q3 (a) List **four(4)** applications of flip-flops/latches.

(4 marks)

(b) For the circuit in **Figure Q3(b):**

(i) State the function of this circuit.

(2 marks)

(ii) Determine the external resistors R1 and R2 to give output frequency of 10kHz with duty cycle of 50% if the external capacitor C is 3nF.

(6 marks)

(c) **Figure Q3(c)** show JK flip-flop configured as a ripple carry up counter.

(i) Draw the timing diagram in **Figure Q3(c).**

(9 marks)

(ii) Modify the circuit to operate as MOD 6 counter.

(4 marks)

Q4 (a) **Figure Q4(a)** shows the block diagram of a 4-bit counter. Show how it can be configured as the following counter. Shows all steps and if the input frequency is 200kHz determine each of the counter output frequency.

(i) MOD 10 counter
(ii) MOD 11 counter
(iii) MOD 14 counter

(15 marks)

(b) For the **Figure Q4(b)**, the propagation delay, t_{pd} for each flip-flop is 40ns and t_{pd} for AND gate is 10ns.

(i) Determine the maximum input clock frequency (f_{max}) for the counter.

(4 marks)

(ii) Determine the maximum input clock frequency (f_{max}) with a MOD-16 ripple counter.

(6 marks)

Q5 (a) A shift register in **Figure 5(a)** has *SHIFT/LOAD* and *CLK* inputs. The serial data input *(SER)* is a 0. The parallel data inputs are *D0* = 1, *D1* = 0, *D2*=1 and *D3*=0 as shown. Develop the data-output waveform in relation to the inputs for Q_0, Q_1, Q_2 and Q_3.

(4 marks)

(b) Several types of architecture are used in PLDs. Draw the block diagram of **three (3)** common types and describe their differences.

(6 marks)

(c) List **five (5)** limitations of PLAs.

(5 marks)

(d) Show how the PLA shown in **Figure Q5(d)** can be configured to implement the following functions. Label all inputs and outputs.

(i) $F1(W,X,Y) = \sum(1,2,3,5,7)$
(ii) $F2(W,X,Y) = \sum(0,4,6,7)$

(10 marks)

Q6 (a) Define each basic memory operations terms below.

(i) Write
(ii) Read.
(iii) Address.

(6 marks)

(b) A certain memory has a capacity of 4K x 8, determine

(i) The number of data inputs and data outputs .
(ii) The number of address lines.
(iii) Its capacity in bytes.

(9 marks)

(c) Define each of the following terms.

(i) RAM

(2 marks)

(iii) ROM

(2 marks)

(iv) EPROM

(3 marks)

(iv) Internal Memory

(3 marks)

- END OF QUESTION –

FINAL EXAMINATION

SEMESTER/SESSION: SEM I/2017/2018 PROGRAMME : 2 DAE
COURSE NAME : LOGIC SYSTEMS COURSE CODE: DAE 21603

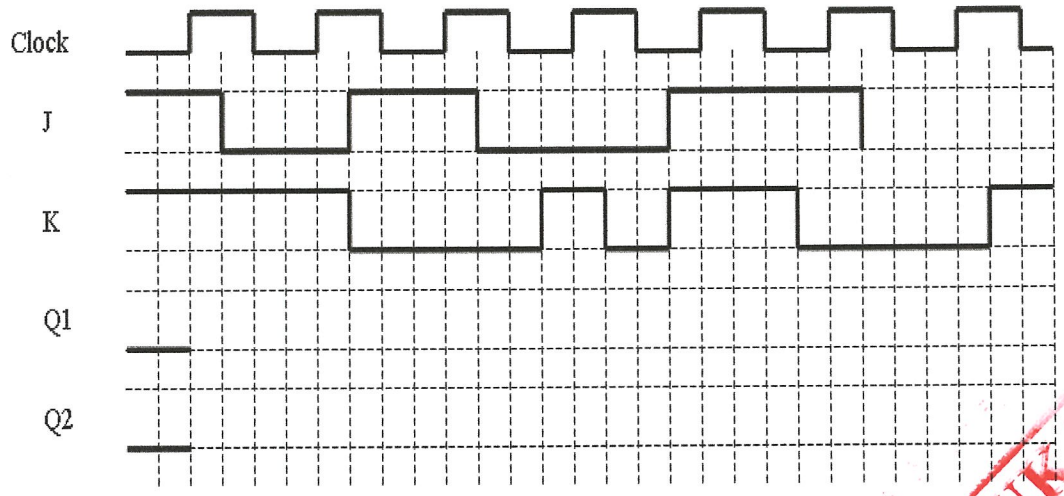

FIGURE Q1(d)

TABLE 1: JK Excitation Table

Q(t)	Q(t+1)	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

FINAL EXAMINATION

SEMESTER/SESSION: SEM I/2017/2018 PROGRAMME : 2 DAE
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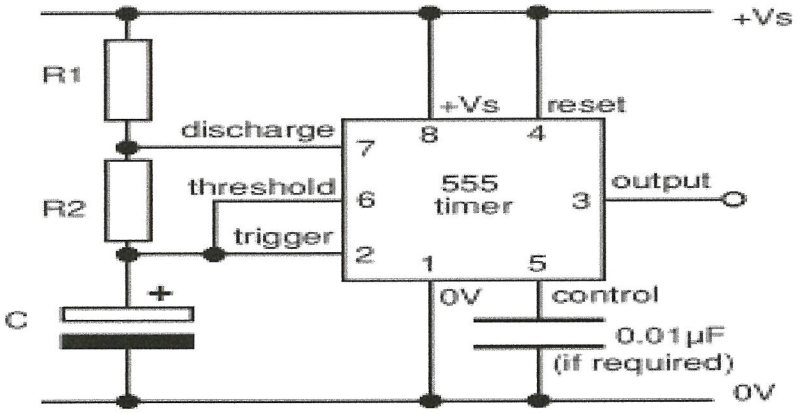


FIGURE Q3(b)

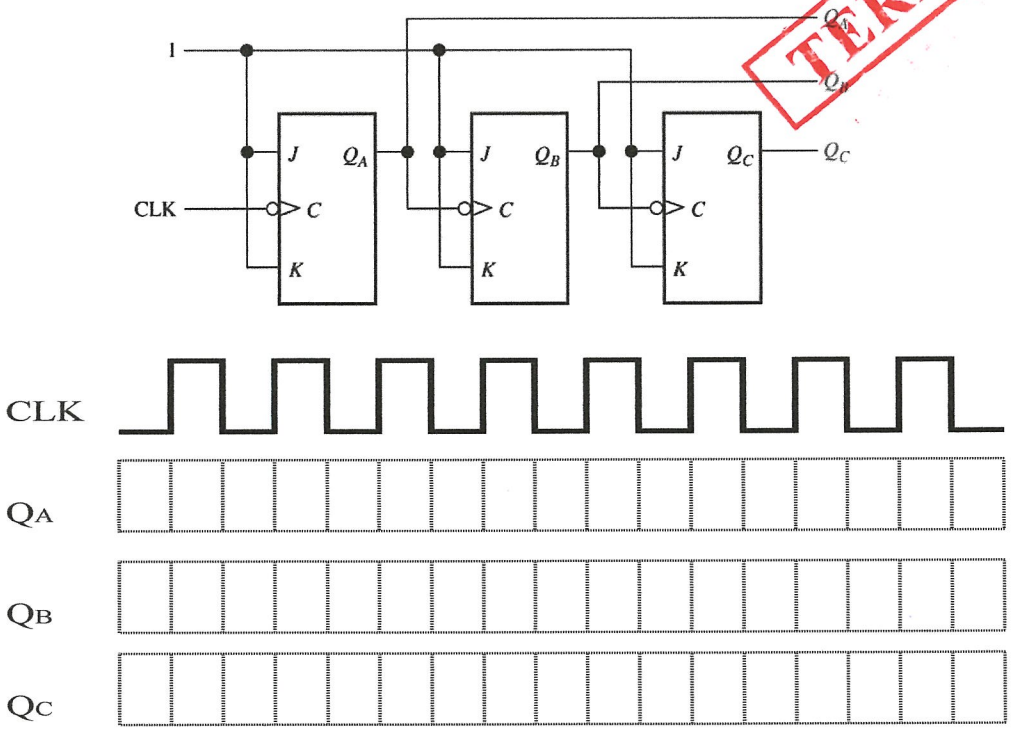
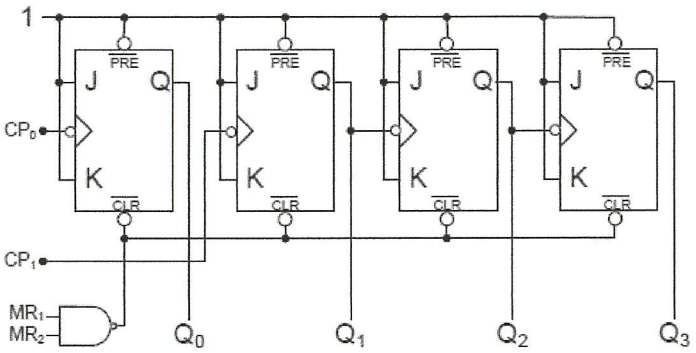


FIGURE Q3(c)

FINAL EXAMINATION

SEMESTER/SESSION: SEM I/2017/2018 PROGRAMME : 2 DAE
COURSE NAME : LOGIC SYSTEMS COURSE CODE: DAE 21603



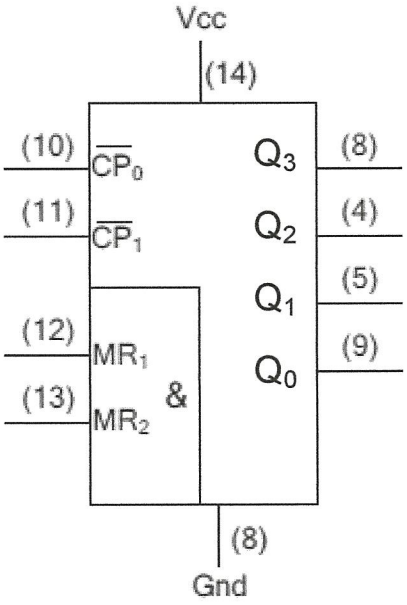


FIGURE Q4(a)

FINAL EXAMINATION

SEMESTER/SESSION: SEM I/2017/2018 PROGRAMME : 2 DAE
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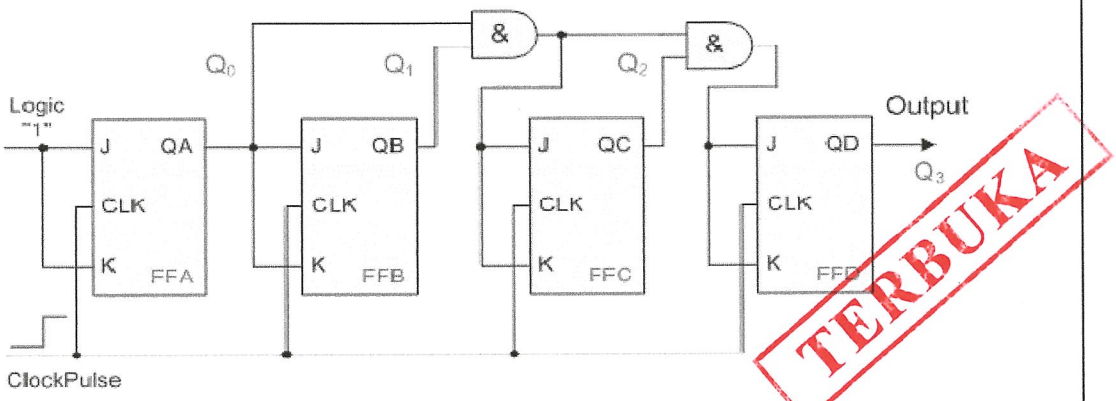

FIGURE Q4(b)

FINAL EXAMINATION

SEMESTER/SESSION: SEM I/2017/2018 PROGRAMME : 2 DAE
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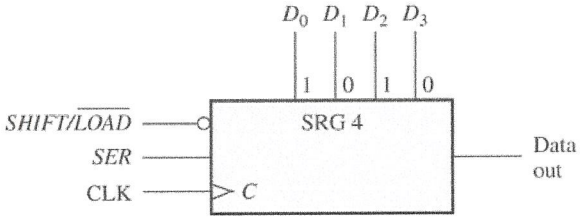

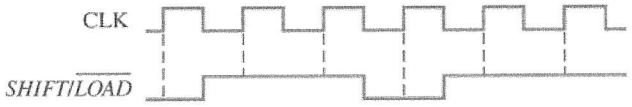

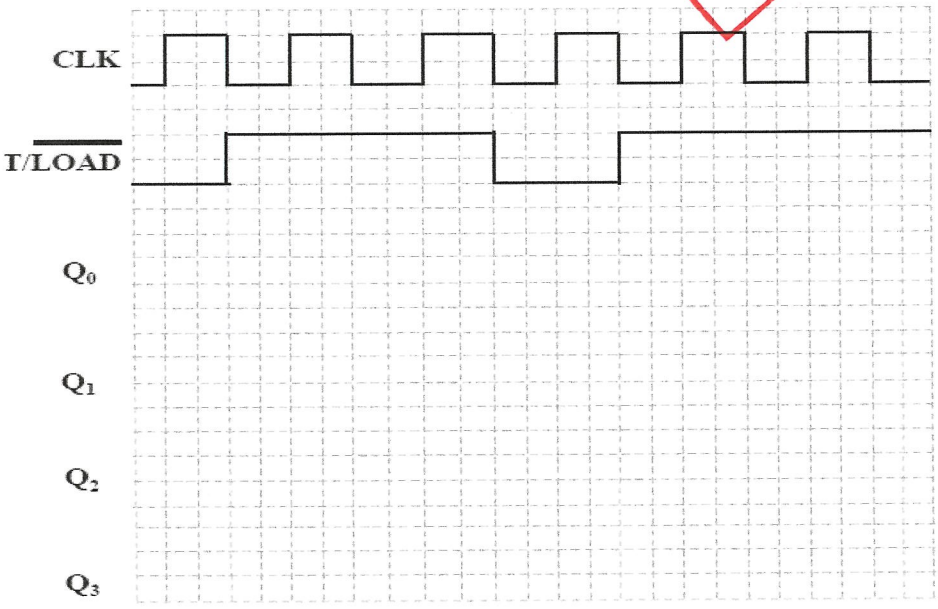

FIGURE Q5(a)

FINAL EXAMINATION

SEMESTER/SESSION: SEM I/2017/2018 PROGRAMME : 2 DAE
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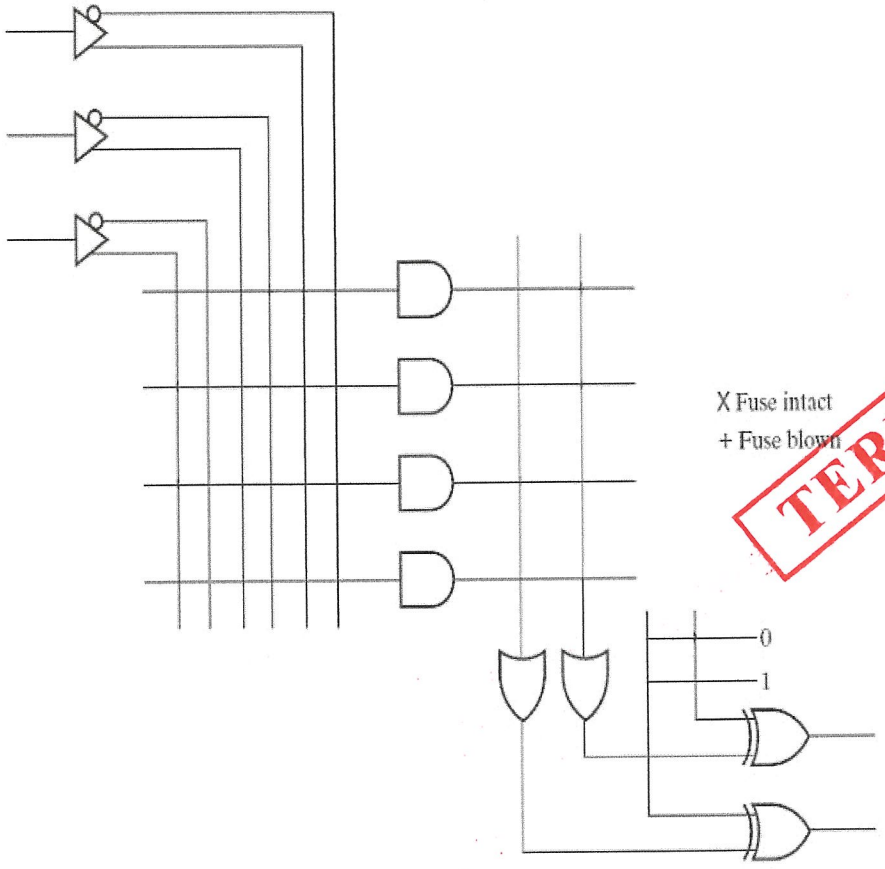

FIGURE Q5(d)