Universiti Tun Hussein Onn Malaysia

UNIVERSITI TUN HUSSEIN ONN MALAYSIA

FINAL EXAMINATION
SEMESTER I
SESSION 2018/2019

COURSE NAME	:	LOGIC SYSTEMS
COURSE CODE	:	DAE 21603
PROGRAMME CODE	:	DAE
EXAMINATION DATE	:	DECEMBER 2018 / JANUARY 2019
DURATION	:	2 HOURS 30 MINUTES
INSTRUCTIONS	:	1) **PART A**: ANSWER ALL QUESTIONS ON OMR PAPER 2) **PART B**: ANSWER **FOUR (4)** QUESTIONS ONLY 3) ATTACH APPENDIX **I, II, III AND IV** WITH YOUR ANSWER BOOKLET

THIS QUESTION PAPER CONSISTS OF **FOURTEEN (14)** PAGES

PART A: PLEASE SELECT THE CORRECT ANSWER.ANSWER ALL QUESTIONS ON OMR PAPER. (20 marks)

Q1 Which of the following is correct for a gated D-type flip-flop?

A. The Q output is either SET or RESET as soon as the D input goes HIGH or LOW
B. The output complement follows the input when enabled
C. Only one of the inputs can be HIGH at a time
D. The output toggles if one of the inputs is held HIGH

Q2 What is a trigger pulse?

A. A pulse that starts a cycle of operation
B. A pulse that reverses the cycle of operation
C. A pulse that prevents a cycle of operation
D. None of the above

Q3 When is a flip-flop said to be transparent?

A. When the Q output is opposite the input
B. When the Q output follows the input
C. When you can see through the IC packaging
D. None of the above

Q4 On a positive edge-triggered S-R flip-flop, the outputs reflect the input condition when _____

A. The clock pulse is LOW
B. The clock pulse is HIGH
C. The clock pulse transitions from LOW to HIGH
D. The clock pulse transitions from HIGH to LOW

Q5 Which statement BEST describes the operation of a negative-edge-triggered D flip-flop?

A. The logic level at the D input is transferred to Q on NGT of CLK
B. The Q output is ALWAYS identical to the CLK input if the D input is HIGH
C. The Q output is ALWAYS identical to the D input when CLK = PGT
D. The Q output is ALWAYS identical to the D input

Q6 Which of the following is correct for a D latch?

A. The output toggles if one of the inputs is held HIGH
B. Q output follows the input D when the enable is HIGH
C. Only one of the inputs can be HIGH at a time
D. The output complement follows the input when enabled

Q7 A ripple counter's speed is limited by the propagation delay of:

A. Each flip-flop
B. All flip-flops and gates
C. The flip-flops only with gates
D. Only circuit gates

Q8 A 5-bit asynchronous binary counter is made up of five flip-flops, each with a 12 ns propagation delay. The total propagation delay (tp (total)) is

A. 12 ms
B. 24 ns
C. 48 ns
D. 60 ns

Q9 A sequential circuit design is used to

A. Count up
B. Count down
C. Decode an end count
D. Count in a random order

Q10 As the number of flip flops are increased, the total propagation delay of

A. Ripple counter increases but that of synchronous counter remains the same
B. Both ripple and synchronous counters increase
C. Both ripple and synchronous counters remain the same
D. Ripple counter remains the same but that of synchronous counter increases

Q11 The main difference between a register and a counter is

A. A register has no specific sequence of states
B. A counter has no specific sequence of states
C. A register has capability to store one bit of information but counter has n-bit
D. None of the above

Q12 What is a fusing process?

A. It is a process by which data is passed to the memory
B. It is a process by which data is read through the memory
C. It is a process by which programs are burnout to the diode/transistors
D. None of the above

Q13 What is the major difference between DRAM and SRAM?

A. Dynamic RAMs are always active; static RAMs must reset between data read/write cycles
B. SRAMs can hold data via a static charge, even with power off
C. The only difference is the terminal from which the data is removed—from the
D. FET Drain or Source
E. DRAMs must be periodically refreshed

Q14 Which ROM can be erased by an electrical signal?

A. ROM
B. Mask ROM
C. EPROM
D. EEPROM

Q15 What does the term "random access" mean in terms of memory?

A. Any address can be accessed in systematic order
B. Any address can be accessed in any order
C. Addresses must be accessed in a specific order
D. None of the above

Q16 The inputs in the PLD is given through

A. NAND gates
B. OR gates
C. NOR gates
D. AND gates

Q17 The difference between a PAL & a PLA is

A. PALs and PLAs are the same thing
B. The PAL has a programmable OR plane and a programmable AND plane, while the PLA only has a programmable AND plane
C. The PLA has a programmable OR plane and a programmable AND plane, while the PAL only has a programmable AND plane
D. The PAL has more possible product terms than the PLA

Q18 Dynamic RAM is more preferable than static RAM, why?

A. DRAM is of the lowest cost, lowest density
B. DRAM is of the highest cost, reduced size
C. DRAM is of the lowest cost, highest density
D. DRAM is more flexible and lowest storage capacity

Q19 The advantages of RAMs are

A. Non-destructive read out
B. Fast operating speed
C. Low power dissipation
D. All of the above

Q20 CD-ROM is a

A. Memory register
B. Magnetic memory
C. Semiconductor memory
D. Non-volatile memory

PART B: ANSWER **FOUR (4)** QUESTIONS ONLY

Q1 (a) State the difference between latches and flip-flop operation. (4 marks)

(b) With the aid of truth tables, describe the differences between the following flip-flops.

(i) RS flip flop (3 marks)

(ii) JK flip-flop. (3 marks)

(iii) D flip-flop. (3 marks)

(c) The waveforms for input signals A and B shown in **Figure Q1(c)(i)** are applied to the circuit shown in **Figure Q1(c)(ii)**. Sketch the waveforms of P, Q, R and S of the circuit on **APPENDIX I**. Assumes that initially R=0 and S=1. (7 marks)

Q2 (a) Design a synchronous counter using JK flip-flop to count 4 digits number. The count sequence is 2,0,3,1 and repeat. The JK excitation table is shown 8 in **Table 1**. Show all steps and the design should include the following :

(i) State diagram (2 marks)

(ii) Excitation table (4 marks)

(iii) K-maps to generate minimal expression (4 marks)

(iv) Circuit implementation (4 marks)

(b) **Figure Q2(b)** shown an astable multivibrator circuit using 555 timer. Determine the external resistors R1 and R2 to give output frequency of 10 kHz with duty cycle of 50 % if the external capacitor C is 3nF. (6 marks)

Q3 (a) State **four (4)** modes of data movement in shift register. (4 marks)

(b) (i) Draw a logic diagram for a 4-bit serial load shift register (SISO) constructed from edge-triggered D-type flip- flops. All the input and output must be labelled completely. (5 marks)

(ii) Explain how the shift register in **Q3(b)(i)** can be cleared. (3 marks)

(iii) For shift register in **Q3(b)(i),** on the successive rising edges of the clock signal CLK, if the input takes on the values 1 0 1 0, show the contents of the shift register after each edge of the clock until 8th clock pulses in table provided in **APPENDIX II**. You may assume that the register contains all zeroes initially.

(8 marks)

Q4 (a) With the aid of diagram, explain the difference between the synchronous and asynchronous counters.

(4 marks)

(b) **Figure Q4(b)(i)** shows the block diagram of a 4-bit counter. Show how it can be configured as the following counter. You may refer to **Figure Q4 (b)(ii)** for its internal circuitry. Draw the following counter circuit on **APPENDIX III.**

(i) MOD 6 (5 marks)

(ii) MOD 13 (5 marks)

(c) For the **Figure Q4(c)**, the propagation delay, t_{pd} for each flip-flop is 40ns and t_{pd} for AND gate is 10ns. Determine the maximum input clock frequency (f_{max}) with a MOD-16 ripple counter.

(6 marks)

Q5 (a) Several types of architecture are used in PLDs. Draw the block diagram of **three (3)** common types and describe their differences.

(12 marks)

(b) Show how the PLA shown in **Figure Q5(b)** can be configured to implement the functions in (i) and (ii). Draw the circuit on **APPENDIX IV**. Label all inputs and outputs.

(i) $F1(W,X,Y) = \Sigma(1,2,3,5,7)$

(4 marks)

(ii) $F2(W,X,Y) = \Sigma(0,4,6,7)$

(4 marks)

Q6 (a) Define each basic memory operation terms below.

(i) Write (2 marks)

(ii) Read (2 marks)

(iii) Address (2 marks)

(b) A certain memory has a capacity of 4K x 8, determine

(i) The number of data inputs and data outputs. (2 marks)

(ii) The number of address lines. (2 marks)

(iii) Its capacity in bytes. (2 marks)

(c) Define each of the following terms.

(i) RAM (2 marks)

(ii) ROM (2 marks)

(iii) EPROM (2 marks)

(iv) Internal Memory (2 marks)

-END OF QUESTIONS –

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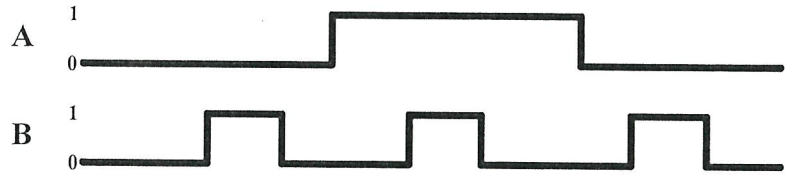

Figure Q1(c)(i)

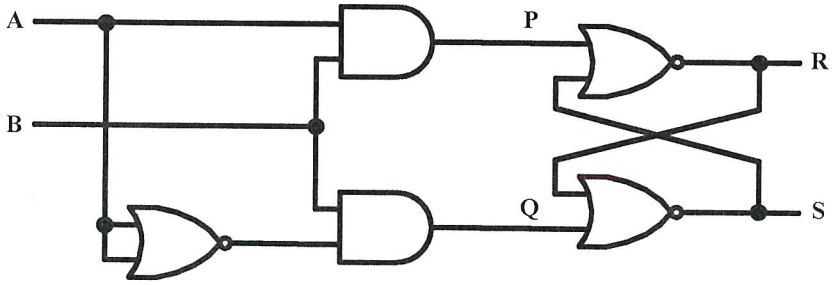

Figure Q1(c)(ii)

Table 1 : JK FF's Excitation Table

Q(t)	Q(t+1)	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

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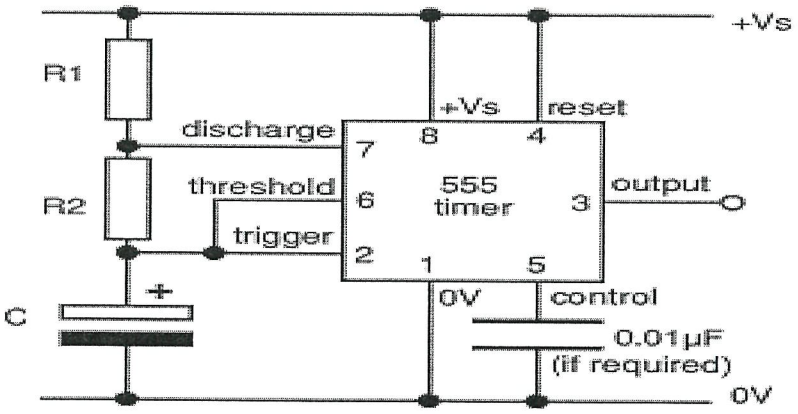
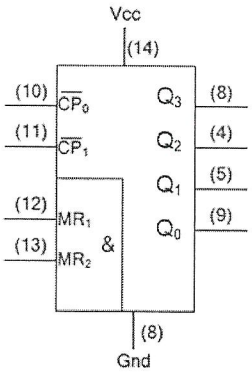
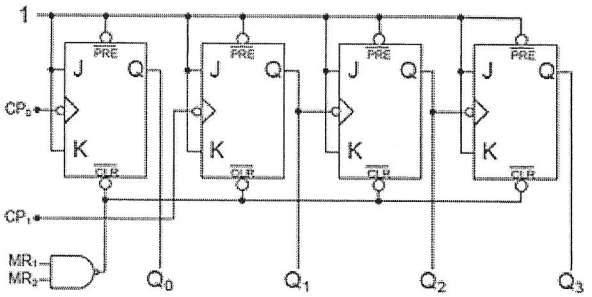


Figure Q2 (b)



(i)



(ii)

Figure Q4 (b)

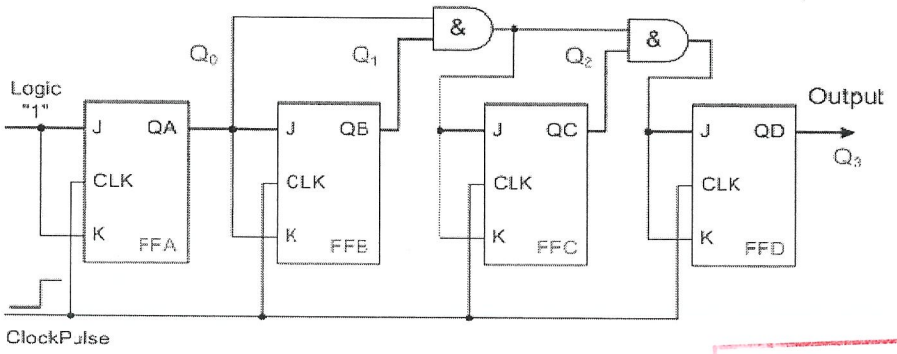


Figure Q4 (c)

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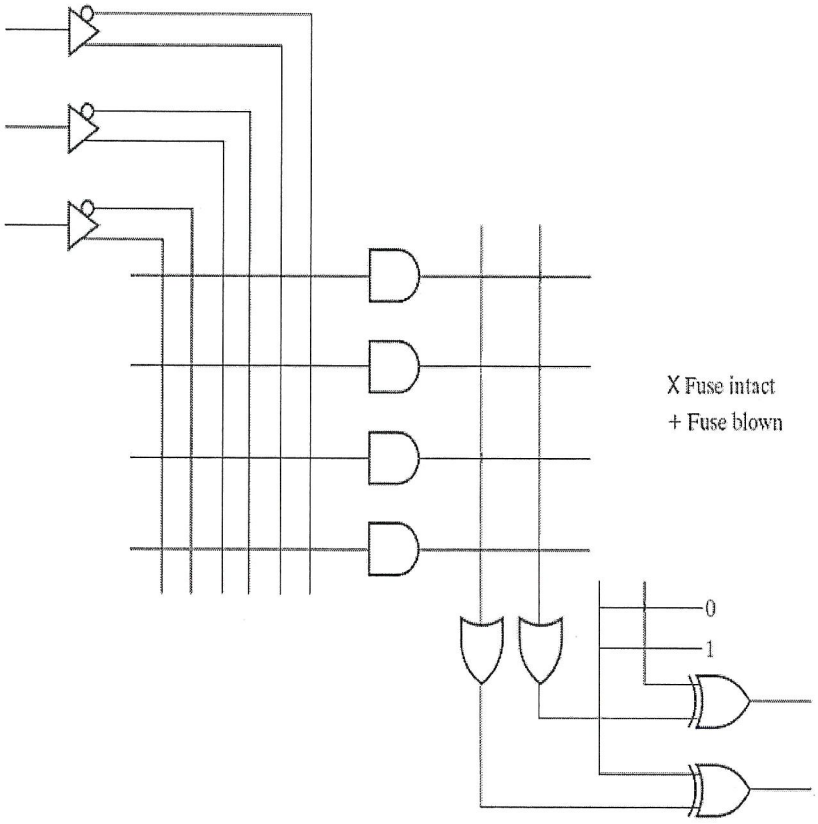

Figure Q5 (b)

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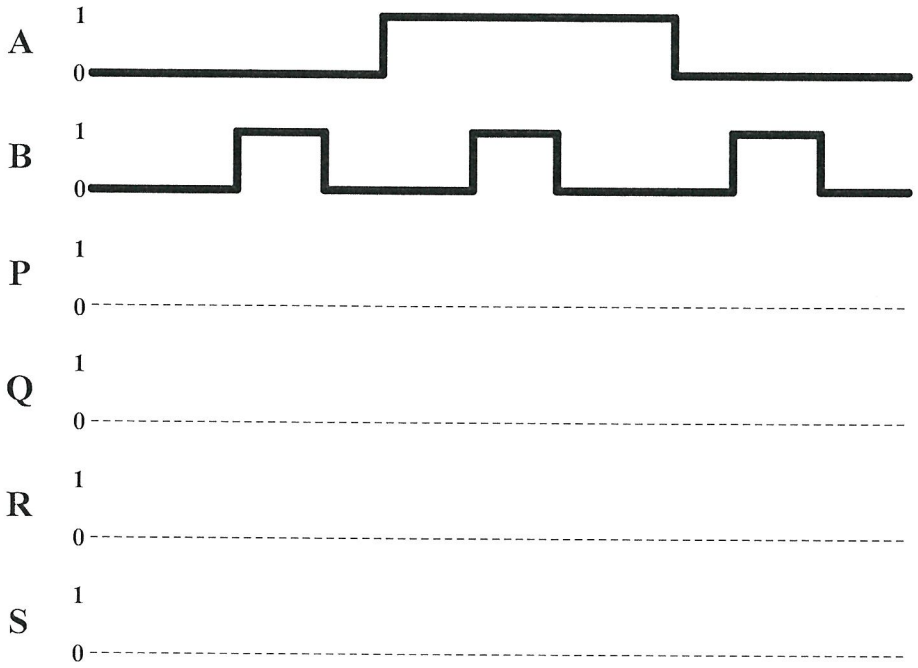
APPENDIX I



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APPENDIX II

Clock Pulse	Q_3	Q_2	Q_1	Q_0
1st				
2nd				
3rd				
4th				
5th				
6th				
7th				
8th				

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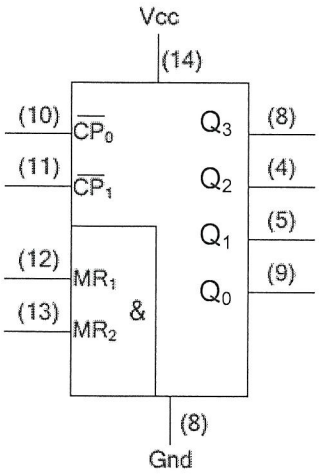
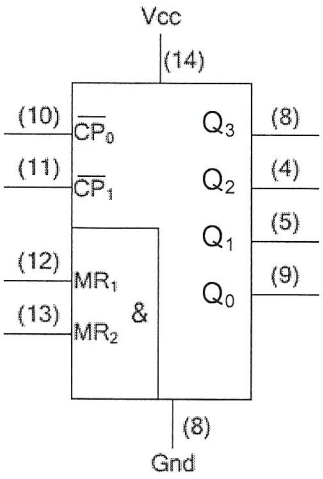
APPENDIX III



MOD 6



MOD 13

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APPENDIX IV