

CONFIDENTIAL



UNIVERSITI TUN HUSSEIN ONN MALAYSIA

**FINAL EXAMINATION
SEMESTER II
SESSION 2018/2019**

COURSE NAME : COMPUTER ARCHITECTURE /
FUNDAMENTAL OF COMPUTER
ARCHITECTURE

COURSE CODE : DAT 10703 / DAT 10403

PROGRAMME CODE : DAT

EXAMINATION DATE : JUNE / JULY 2019

DURATION : 2 HOURS 30 MINUTES

INSTRUCTION : ANSWERS ALL QUESTIONS.

THIS QUESTION PAPER CONSISTS OF ELEVEN (11) PAGES

CONFIDENTIAL

PART A

- Q1** The following interface are application of bus system **EXCEPT**
- A. Acceralated Graphic Port (AGP).
 - B. Universal Serial Bus (USB).
 - C. Serial Advanced Technology Attachment (SATA).
 - D. Peripheral Component Interconnect (PCI).
- Q2** Which following components are the components in the Computer Processing Unit (CPU)?
- I Pointer Counter (PC).
 - II Arithmetic Logic Unit (ALU).
 - III Control Unit (CU).
 - IV Register.
- A. I & II
 - B. I, II & III
 - C. II, III & IV
 - D. All of the above.
- Q3** What is the function of Data line in the bus structure?
- A. control signals transmit both control command and timing information between system modules.
 - B. provide a path for moving data between system modules.
 - C. designate source and destination of the data in the bus system.
 - D. determine access to and the use data.
- Q4** Which component determine the width of bus system?
- A. data Line.
 - B. address Line.
 - C. control Line.
 - D. front Line.
- Q5** In the basic instruction cycle, the program execution will be halt only if below condition occurs **EXCEPT**
- A. The computer is turn on.
 - B. The computer is accidentally shut down.
 - C. Unrecoverable error occurs.
 - D. The program instruct that halt the computer is encounter.

- Q6** Peripheral device is a device designated to
- A. coordinate the flow of traffic between internal resources and external devices.
 - B. exchange data between the processor and the I/O modules via bus system.
 - C. connect an external device with I/O module interface.
 - D. perform communication between CPU and computer memory.
- Q7** External devices can be categorized into
- I Human readable.
 - II Machine readable.
 - III Communication.
 - IV Interconnection.
- A. I & II
 - B. I, II & III
 - C. II, III & IV
 - D. All of the above.
- Q8** Which the following devices are external device?
- I RFID tag.
 - II Video Display Terminal.
 - III Solid State Drive.
 - IV Network Interface Card.
- A. I & II
 - B. I, II & III
 - C. II, III & IV
 - D. All of the above.
- Q9** Keyboard provides _____ that is transmitted to the computer.
- A. device
 - B. signal
 - C. output
 - D. input
- Q10** Which the following file formats are using in the Unicode Transformation Format (UTF)?
- I UTF 64
 - II UTF 32
 - III UTF 16
 - IV UTF 8
- A. I & II
 - B. I, II & III
 - C. II, III & IV
 - D. All of the above.

- Q11** Below are techniques used in the operation of input/output **EXCEPT**
- A. Programmed I/O.
 - B. Interface I/O.
 - C. Input Driven I/O.
 - D. Direct Memory Access.
- Q12** Which instruction involves during communication between processor and input/output interface?
- A. Command encoding.
 - B. Control signal.
 - C. I/O interrupt module.
 - D. Status report.
- Q13** Computer organization can be defined as
- A. attributes of a system visible to a programmer.
 - B. the operational unit and their interconnection that realise the architectural specification.
 - C. a set of discipline that describes a computer system by specifying it's part and their relation.
 - D. a specifications detailing how a set of software and hardware standard interact to form a computer.
- Q14** What is the most innovative invention in the second generation computer?
- A. Vacuum Tube.
 - B. Resistor.
 - C. Transistor.
 - D. Diode.
- Q15** What is the first operational stored-program computer using Von Neumann architecture?
- A. Electronic Numerical Integrator and Computer (ENIAC).
 - B. Electronic Discrete Variable Computer (EDVAC).
 - C. Electronic Delay Storage Automatic Calculator (EDSAC).
 - D. Electronic Digital Universal Computing (EDUCE).

Q16 What are the disadvantages of the Fourth Generation computer compare to the previous generation?

- I Require complicated technology to bind chip on the board.
- II The working of computer is still depending on the instructions given by programmer.
- III Computer still require to place in air conditioned place.
- IV The storage capacity of computer still small.

- A. I & II
- B. I, II & III
- C. II, III & IV
- D. All of the above.

Q17 An interconnected set of logic gate can be represented through

- I Boolean Equation.
- II Graphical symbols.
- III Truth table.
- IV IPO table.

- A. I & II
- B. I, II & III
- C. II, III & IV
- D. All of the above.

Q18 What is the logic gate can be represented from the truth table in **Figure Q18**?

- A. NOR
- B. NAND
- C. NOT
- D. XOR

Q19 The circuit in **Figure Q19** shows a circuit that will switch on the lamp IF and ONLY IF switch A and B is ON.

What is the equivalence logic circuit for **Figure Q19**?

- A. OR
- B. AND
- C. NOT
- D. XOR

Q20 What is the function of analog to digital converter (ADC)?

- A. Collect analog signal from real world to the machine.
- B. Store analog signal before process into desired output.
- C. Translate real world signal into digital technology.
- D. Convert digital signal into analog signal.

Q21 A user-visible register can be categorized as below

- I General purpose
- II Data
- III Address
- IV Condition codes

- A. I & II
- B. I, II & III
- C. II, III & IV
- D. All of the above.

Q22 What is the function of Program Status Word (PSW)?

- A. Collected information from a register or a set of register.
- B. Contain status information.
- C. Interpreted opcode and execute information from register.
- D. To hold data from program counter.

Q23 Which the following instructions are part of basic instruction cycle?

- I Fetch instructions.
- II Fetch data.
- III Write data.
- IV Interrupt data.

- A. I & II
- B. I, II & III
- C. II, III & IV
- D. All of the above.

Q24 What is the roles of the register in the processor?

- I User-visible registers.
- II Control and status registers.
- III General purpose register.
- IV Instruction register.

- A. I & II
- B. I, II & III
- C. II, III & IV
- D. All above

Q25 What will be happened if the interrupt is enable in the instruction cycle?

- A. Opcode will be interpreted and the indicated instruction will be performing.
- B. Instruction cycle will be halt and next instruction will be fetched.
- C. The next instruction will be load from memory into processor.
- D. The current process will be saved and service is interrupted.

PART B

- Q26** (a) Briefly explain **THREE (3)** memory access methods with example. (9 marks)
- (b) Cache memory is smaller than internal memory but faster in term of transfer rate. Therefore, cache memory capacity is easy to full and some of the cached blocks need to be removed before bringing new ones in.
- (i) Discuss on how to increase the performance by using cache memory. (3 marks)
- (ii) Briefly explain **TWO (2)** cache replacement policy to avoid situation above. (2 marks)
- (c) **Figure Q26(a)** and **Figure Q26(b)** show the C programming coding with the expected result.
- (i) Discuss application of temporal locality and spatial locality based on data and instruction in **Figure Q26(a)** and **Figure Q26(b)**. (4 marks)
- (ii) Evaluate which coding are faster in term of access time. (1 mark)
- (iii) Explain your reason to support the decision in **Q26(b)(ii)** (2 marks)
- (d) Consider a memory cache with a block size of 8 words. It takes 2 clock cycle to access a word in cache and takes 15 clock cycles to access a word from RAM.
- (i) Determine how much time to take to access a word that's not in cache.
- (ii) Calculate the average memory access time if miss rate is 20%? (4 marks)

Q27 (a) (i) Briefly discuss each type of the computer language. (6 marks)

(ii) Describe the relationship between high level language and machine language with example. (6 marks)

(b) Given the following registers in the Arithmetic and Logic Unit (ALU):

R1	1	0	1	0	0	1	1	0
R2	0	0	1	0	0	1	0	0

Determine output of register after the following instructions are executed.

(i) ADD R2, R1 (2 marks)

(ii) MOV R1, R2 (1 mark)

(iii) ORL R1, R2 (2 marks)

(c) Interpret the meaning of the following assembly code statements.

(i) ANL A, #55H
 (ii) DIV R1, R2 (4 marks)

(d) Given the C programming code as below

$$m = (b + c) - d$$

Using Accumulator and Register, translate C programming above into the assembler language. (4 marks)

- Q28** (a) Describe application of each encoding format in Unicode. (6 marks)
- (b) Convert a hexadecimal number $F1516_{16}$ into the following number systems. Show all your working steps.
- (i) Binary number (base-2). (2 marks)
- (ii) Octal number (base-8). (3 marks)
- (iii) decimal number (base-10). (4 marks)
- (c) Given a decimal problem as below
- $$y = 0.405 \div 3 \times (4 + 2)$$
- Convert y into the following number system:
- (i) Binary number (base-2). (4 marks)
- (ii) Octal number (base-8). (3 marks)
- (iii) Hexadecimal number (base-16). (3 marks)

-END OF QUESTIONS –

FINAL EXAMINATION

SEMESTER / SESSION: SEM II / 2018/2019
COURSE NAME: COMPUTER ARCHITECTURE

PROGRAMME CODE : DAT
COURSE CODE : DAT 10703 / DAT 10403

Input		Output
A	B	X
0	0	1
0	1	0
1	0	0
1	1	0

Figure Q18

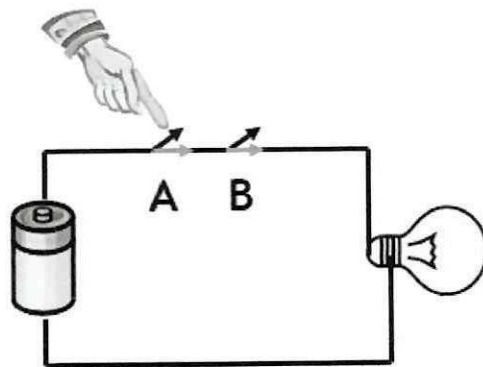


Figure Q19

FINAL EXAMINATION

SEMESTER / SESSION: SEM II / 2018/2019
 COURSE NAME: COMPUTER ARCHITECTURE

PROGRAMME CODE : DAT
 COURSE CODE : DAT 10703 / DAT 10403

Coding	Output																
<pre>sum = 0; m=3; n=3; for (i = 0; i < n; i++) for (j = 0; j < m; j++) sum += a[i][j]; return sum;</pre>	<table border="1"> <thead> <tr> <th></th> <th>Col 1</th> <th>Col 2</th> <th>Col 3</th> </tr> </thead> <tbody> <tr> <th>Row 1</th> <td>1,1</td> <td>1,2</td> <td>1,3</td> </tr> <tr> <th>Row 2</th> <td>2,1</td> <td>2,2</td> <td>2,3</td> </tr> <tr> <th>Row 3</th> <td>3,1</td> <td>3,2</td> <td>3,3</td> </tr> </tbody> </table>		Col 1	Col 2	Col 3	Row 1	1,1	1,2	1,3	Row 2	2,1	2,2	2,3	Row 3	3,1	3,2	3,3
	Col 1	Col 2	Col 3														
Row 1	1,1	1,2	1,3														
Row 2	2,1	2,2	2,3														
Row 3	3,1	3,2	3,3														

Figure Q26(a)

Coding	Output									
<pre>sum = 0; m=1; n=9; for (j = 0; j < m; j++) for (i = 0; i < n; i++) sum += a[i][j]; return sum;</pre>	<table border="1"> <tr> <td>1,1</td> <td>1,2</td> <td>1,3</td> <td>2,1</td> <td>2,2</td> <td>2,3</td> <td>3,1</td> <td>3,2</td> <td>3,3</td> </tr> </table>	1,1	1,2	1,3	2,1	2,2	2,3	3,1	3,2	3,3
1,1	1,2	1,3	2,1	2,2	2,3	3,1	3,2	3,3		

Figure Q26(b)