Universiti Tun Hussein Onn Malaysia

UNIVERSITI TUN HUSSEIN ONN MALAYSIA

FINAL EXAMINATION
SEMESTER II
SESSION 2016/2017

COURSE NAME	:	ELECTRONICS I
COURSE CODE	:	BWC 10703
PROGRAMME CODE	:	BWC
EXAMINATION DATE	:	JUNE 2017
DURATION	:	3 HOURS
INSTRUCTION	:	ANSWERS **ALL** QUESTIONS

THIS QUESTION PAPER CONSISTS OF **FIVE (5)** PAGES

Q1 (a) Describe Kirchoff's Voltage Law

(2 marks)

(b) As to **Figure Q1(b)** is considered,
(i) determine V_2 using KVL
(ii) calculate I
(iii) find R_1 and R_3

(8 marks)

(c) For the network of **Figure Q1(c)**, by using voltage divider rule
(i) calculate V_{ab}
(ii) determine V_b
(iii) calculate V_c

(10 marks)

Q2 (a) State the The'venin's Theorem

(2 marks)

(b) Find the The'venin equivalent circuit for in the shaded area of the network in **Figure Q2(b)**

(10 marks)

(c) (i) What is a semiconductor? How it can be compared with a conductor and an insulator?
(ii) Describe forward and reverse biased of a diode
[Diagrams might help in these questions]

(8 marks)

Q3 **Figure Q3** shows the full wave rectifier circuit. T_1 is a step down transformer, which provides the secondary voltage. This transformer secondary is called as center tapped. In this figure, each half of the secondary has a voltage of 15 V_{ac}, which is one half the total secondary voltages, V_S, of 30 V_{ac}. The voltage for the top half of the secondary is designated V_1, whereas the voltage for the bottom half of the secondary is designated V_2. Analyze;

(a) top half of secondary voltage V_1,

(6 marks)

(b) bottom half of secondary voltage, V_2,

(2 marks)

(c) output voltage produced when D_1 is conducted.

(4 marks)

(d) output voltage produced when D_2 is conducted.

(2 marks)

(e) the combination output voltage produced by D_1 and D_2 and value of I_L.

(6 marks)

Q4 (a) Explain the function of emitter and collector regions in a transistor.

(2 marks)

(b) For the circuit shown in **Figure Q4(b)**, calculate the value for V_B, V_E, I_C, V_{CE}, $I_{C(sat)}$ and $V_{CE(off)}$. Then, construct a dc load line showing the value of $I_{C(sat)}$, $V_{CE(off)}$, I_{CQ} and V_{CEQ}.

(18 marks)

Q5 (a) Draw the schematic symbol of JFETs
(i) n-channel symbol
(ii) offset-gate symbol
(iii) p-channel symbol

(6 marks)

(b) Assume that the JFET circuit in **Figure Q5(b)** is to be mass produced. The JFET has the following parameters:

Parameter	Minimum	Maximum
I_{DSS}	2 mA	20 mA
$V_{GS(off)}$	-2 V	-8 V

Calculate the minimum and maximum value for I_D and V_{DS} if V_{GS} = -1.5 V for the range of JFET parameters shown and conclude the finding.

(14 marks)

– **END OF QUESTIONS** –

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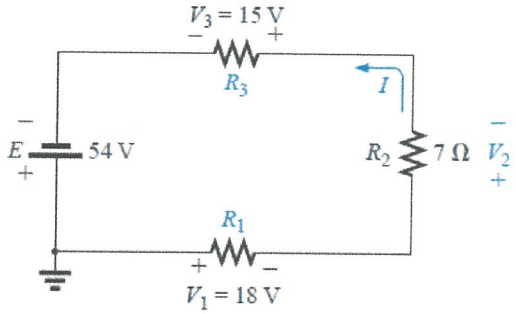

Figure Q1(b)

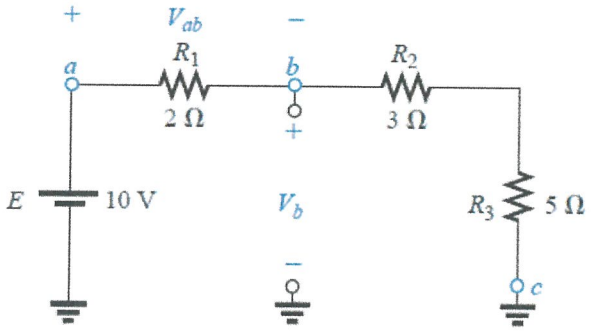

Figure Q1(c)

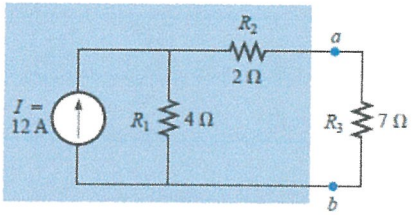

Figure Q2(b)

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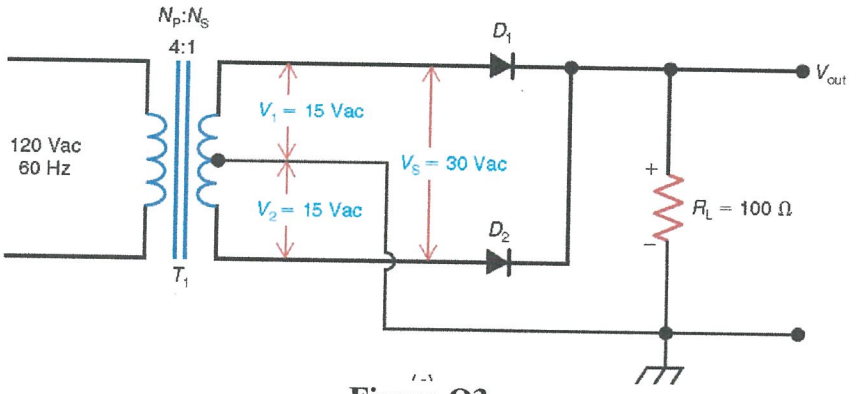

Figure Q3

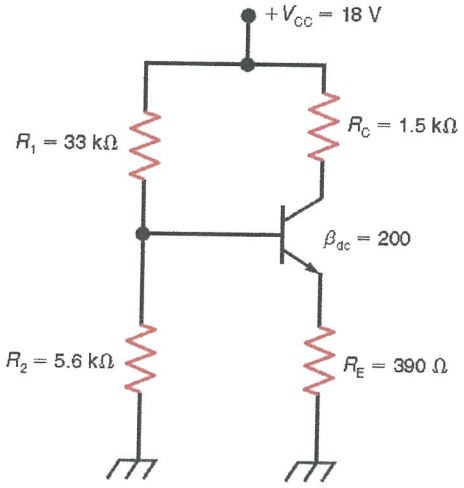

Figure Q4(b)

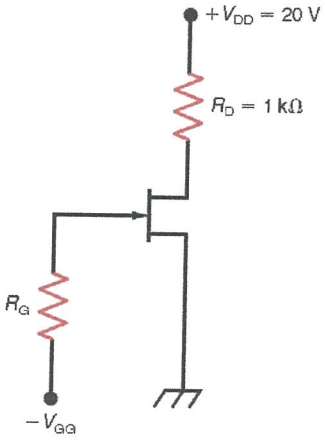

Figure Q5(b)