UTHM
Universiti Tun Hussein Onn Malaysia

UNIVERSITI TUN HUSSEIN ONN MALAYSIA

FINAL EXAMINATION
SEMESTER I
SESSION 2017/2018

COURSE NAME	:	COMPUTER ARCHITECTURE
COURSE CODE	:	BNR 31803
PROGRAMME	:	BNF
EXAMINATION DATE	:	DECEMBER 2017 / JANUARY 2018
DURATION	:	3 HOURS
INSTRUCTION	:	ANSWER **ALL** QUESTIONS

THIS QUESTION PAPER CONSISTS OF **FIVE (5)** PAGES

Q1 (a) Explain Moore's Law. (4 marks)

(b) Consider two different machines, with two different instruction sets, both of which having a clock rate of 200 MHz. The measurements in **Table Q1(b)** are recorded on the two machines running a given set of benchmark programs. Given

$$CPI = \frac{\sum_{i=1}^{n}(CPI_i \times I_i)}{I_c}$$

$$MIPS\ rate = \frac{I_c}{T \times 10^6} = \frac{f}{CPI \times 10^6}$$

(i) Determine the effective CPI, MIPS rate, and execution time for each machine. (6 marks)

(ii) Analyse the results. (2 marks)

(c) Four benchmark programs are executed on three computers. **Table Q1(c)** shows the execution time in seconds, with 100,000,000 instructions executed in each of the four programs. Calculate the MIPS values for each computer for each program. Then, calculate the arithmetic and harmonic means assuming equal weights for the four programs, and rank the computers based on arithmetic mean and harmonic mean. (8 marks)

Q2 (a) Discuss the differences among direct mapping, associative mapping, and set associative mapping. (6 marks)

(b) A set-associative cache consists of 64 lines, or slots, divided into four-line sets. Main memory contains 4K blocks of 128 words each. Show the format of main memory addresses. (4 marks)

(c) Consider a machine with a byte addressable main memory of 2^{16} bytes and block size of 8 bytes. Assume that a direct mapped cache consisting of 32 lines is used with this machine.

(i) Show how is a 16-bit memory address divided into tag, line number, and byte number. (2 marks)

(ii) Determine into what line would bytes with each of the following addresses be stored.

0001 0001 0001 1011
1100 0011 0011 0100
1101 0000 0001 1101
1010 1010 1010 1010

(2 marks)

(iii) Suppose the byte with address 0001 1010 0001 1010 is stored in the cache. Determine the addresses of the other bytes stored along with it. (2 marks)

(iv) Determine the total bytes of memory can be stored in the cache. (2 marks)

(v) Explain why is the tag also stored in the cache. (2 marks)

Q3 (a) Explain Direct Memory Access (DMA) operation.

(4 marks)

(b) Discuss **THREE (3)** functions of Operating System.

(6 marks)

(c) (i) State **FOUR (4)** types of Operating System.

(4 marks)

(ii) Differentiate between single programming operation and multi-programming operation. Sketch the diagram.

(6 marks)

Q4 (a) Sketch example of 3-bit full adders for addition in computer arithmetic.

(3 marks)

(b) Assume A is 1011 and B is 0011, calculate:

(i) A + B for unsigned addition (2 marks)

(ii) A + B for signed addition (2 marks)

(c) There are **TWO (2)** versions of binary multiplier algorithm.

(i) Differentiate between First Version Multiplier and Second Version Multiplier. Sketch suitable diagram.

(8 marks)

(ii) Assume A is 1011 and B is 0011. Calculate A x B using multiplier algorithm (Second Version)

(5 marks)

Q5 (a) Sketch diagram for instruction sets format and explain briefly each parts.

(3 marks)

(b) Differentiate between Reduced Instruction Set Computer (RISC) and Complex Instruction Set Computer (CISC).

(4 marks)

(c) A RISC machine may do both a mapping of symbolic registers to actual registers and a rearrangement of instructions for pipeline efficiency. An interesting question arises as to the order in which these two operations should be done. Consider the following program fragment:

```
LD    SR1,A        ;load A into symbolic register 1
LD    SR2,B        ;load B into symbolic register 2
ADD   SR3,SR1,SR2  ;add contents of SR1 and SR2 and store in SR3
LD    SR4,C        ;load C into symbolic register 4
LD    SR5,D        ;load D into symbolic register 5
ADD   SR6,SR4,SR5  ;add contents of SR4 and SR5 and store in SR6
```

(i) First do the register mapping and then any possible instruction reordering. Determine how many machine registers are used. Based on your codes, has there been any pipeline improvement? Discuss your analysis.

(6 marks)

(ii) Starting with the original program, do instruction reordering and then any possible mapping. Determine how many machine registers are used. Based on your codes, has there been any pipeline improvement? Discuss your analysis.

(7 marks)

- END OF QUESTIONS -

FINAL EXAMINATION

SEMESTER / SESSION : SEM I / 2017/2018
COURSE NAME : COMPUTER ARCHITECTURE
PROGRAMME CODE : BNF
COURSE CODE : BNR 31803

Table Q1(b)

	Instruction Type	Instruction Count (millions)	Cycles per Instruction
Machine A	Arithmetic and logic	8	1
	Load and store	4	3
	Branch	2	4
	Others	4	3
Machine B	Arithmetic and logic	10	1
	Load and store	8	2
	Branch	2	4
	Others	4	3

Table Q1(c)

Type of Program	Computer A	Computer B	Computer C
Program 1	1	10	20
Program 2	1000	100	20
Program 3	500	1000	50
Program 4	100	800	100