UNIVERSITI TUN HUSSEIN ONN MALAYSIA

PEPERIKSAAN AKHIR
SEMESTER II
SESI 2008/09

NAMA MATA PELAJARAN	:	SISTEM LOGIK
KOD MATAPELAJARAN	:	DEE 2223
KURSUS	:	2 DET / DEE / DEX
TARIKH PEPERIKSAAN	:	APRIL 2009
JANGKA MASA	:	3 JAM
ARAHAN	:	**BAHAGIAN A** : JAWAB **SEMUA** SOALAN **BAHAGIAN B** : JAWAB **TIGA (3)** SOALAN SAHAJA DARIPADA **LIMA (5)** SOALAN.

KERTAS SOALAN INI MENGANDUNGI 17 MUKA SURAT

PART A

Q1 (a) Draw an active HIGH input R-S latch logic diagram and build its truth table.

(3 marks)

(b) Modify the logic diagram that you have drawn in part Q1(a) if a signal ENABLE is applied.

(2 marks)

(c) State the name of the new logic circuit that you have drawn in part Q1(b)?

(1 marks)

(d) Sketch the Q output waveform for the logic diagram from part Q1(b), when input waveforms EN, S and R as shown in Figure Q1(d) are applied.

(2 marks)

Q2 (a) Draw a logic diagram for four-bit asynchronous binary counter using negative edge-triggered J-K flip-flop and sketch the complete timing diagram using CLK input in Figure Q2(a).

(3 marks)

(b) Determine the maximum clock frequency at which the counter can be operated for a 4-bit asynchronous binary counter if each negative edge-triggered flip-flop has a propagation delay for 15ns.

(2 marks)

(c) Draw a logic diagram for four-bit synchronous binary counter using positive edge-triggered flip-flop and sketch the complete timing diagram using CLK input in Figure Q2(c).

(3 marks)

Q3 (a) Draw the logic symbol for a positive edge-triggered S-R and J-K flip-flop.

(2 marks)

(b) What is the difference between a latch and a flip-flop? Give one reason and one example using logic symbol.

(2 marks)

(c) Show how a negative Edge Triggered D Flip-Flop can be implemented using an S-R flip-flop and inverter.

(1 marks)

(d) The input waveforms in Figure Q3(d) are applied to CLK, D, PRE and CLR as indicated. Determine and draw the $\overline{Q}$ output waveform.

(3 marks)

Q4 (a) State **THREE** (3) possible mode of register operation.

(3 marks)

(b) The circuit shown in Figure Q4(b)(i) is a 5 bits universal register. Sketch all the parallel output Q_0,Q_1,Q_2,Q_3 and Q_4 waveforms in Figure Q4(b)(ii), the states of the 5-bit register (SRG 5), if the data input given is 01101 and clock waveforms as shown in Figure Q4(b)(ii). The register initially contains all 0s.

(5 marks)

Q5 (a) Show how a NOR gate can be implemented by using only four NAND gates.

(3 marks)

(b) Show how a AND gate can be implemented by using only three NOR gates.

(3 marks)

(c) Sketch the output waveform, X for the circuit shown in Figure Q5(c), by referring to the given input waveforms A, B and C and output waveform Y.

(2 marks)

PART B (Show all your steps)

Q6 (a) Determine the Boolean expression of X for the circuit shown in Figure Q6(a).
(4 marks)

(b) Convert the Boolean expression from part Q6(a) into a standard SOP expression.
(6 marks)

(c) Use Karnaugh map to determine the minimum SOP expression for X.
(10 marks)

Q7 (a) With the 555 Timer IC and RC component, draw the complete schematic diagram for monostable (one-shot) operation and astable operation.
(6 marks)

(b) Determine the time width (t_w) for monostable (One-Shot) if given E = 90V, R = 9kΩ and C = 10nF
(3 marks)

(c) Determine the external capacitor (C_{ext}) for monostable (One-Shot) if given E = 12V, t_w = 0.5s and R = 40kΩ
(3 marks)

(d) For the astable multivibrator, if R_1=1MΩ, R_2= 470kΩ and C_1=0.001uF, determine the frequency output, t_{HI}, t_{LO} and duty cycle, also draw the output waveform at pin 3.
(8 marks)

Q8 (a) Determine the output Q_0,Q_1,Q_2 and Q_3 of 74HC194 IC a 4-bit bidirectional universal shift register if given the data input waveforms is given as shown in Figure Q8(a).
(14 marks)

(b) If a 10-bit ring counter in Figure Q8(b) has the initial state 0101001111, determine the waveform for each of the Q outputs.
(6marks)

Q9 (a) Convert each of the BINARY code 0000, 0010, 0100, 0110, 0111 to Gray Code.
(3 marks)

(b) Design a J-K synchronous 3-bit up/down counter with a Gray code sequence from Q9(a). The counter should count up when an UP/$\overline{\text{DOWN}}$ control input is 1 and count down when the control input is 0.
(17marks)

Q10 (a) By referring to the logic schematic J-K flip-flop in Figure Q10(a)(i), determine the output $\bar{Q}$ if the input waveforms CLK, J, K, Clear and Preset is given in Figure Q10(a)(ii). Q is initially 1.

(10 marks)

(b) Determine the waveforms at Q, $\bar{Q}$ (Q'), CP and $\overline{CP}$ (CP') in Figure Q10(b) for a non-overlapping clock.

(10 marks)

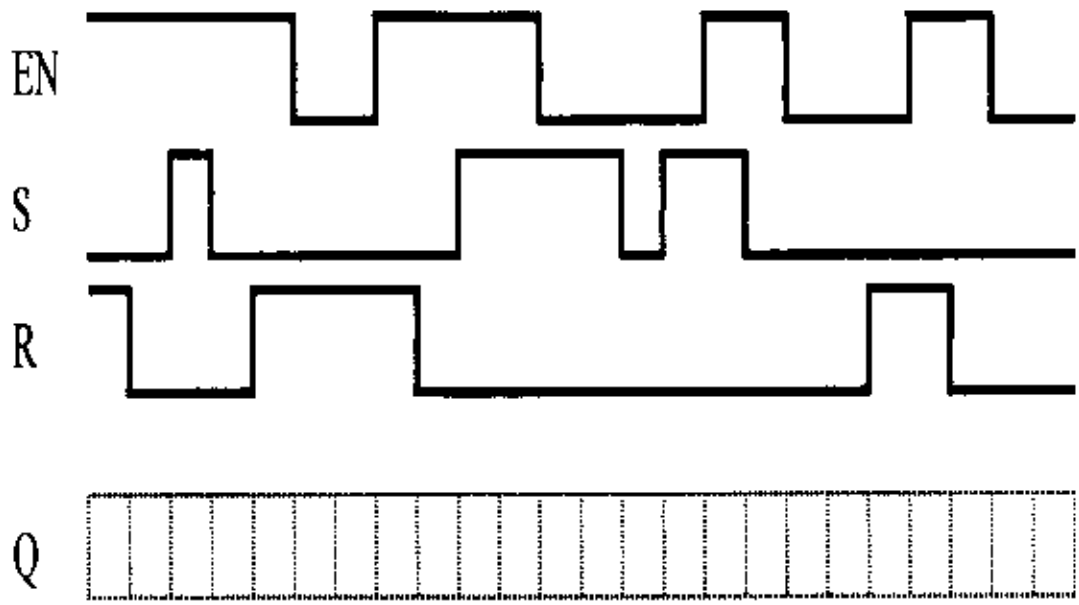


FIGURE Q1(d)

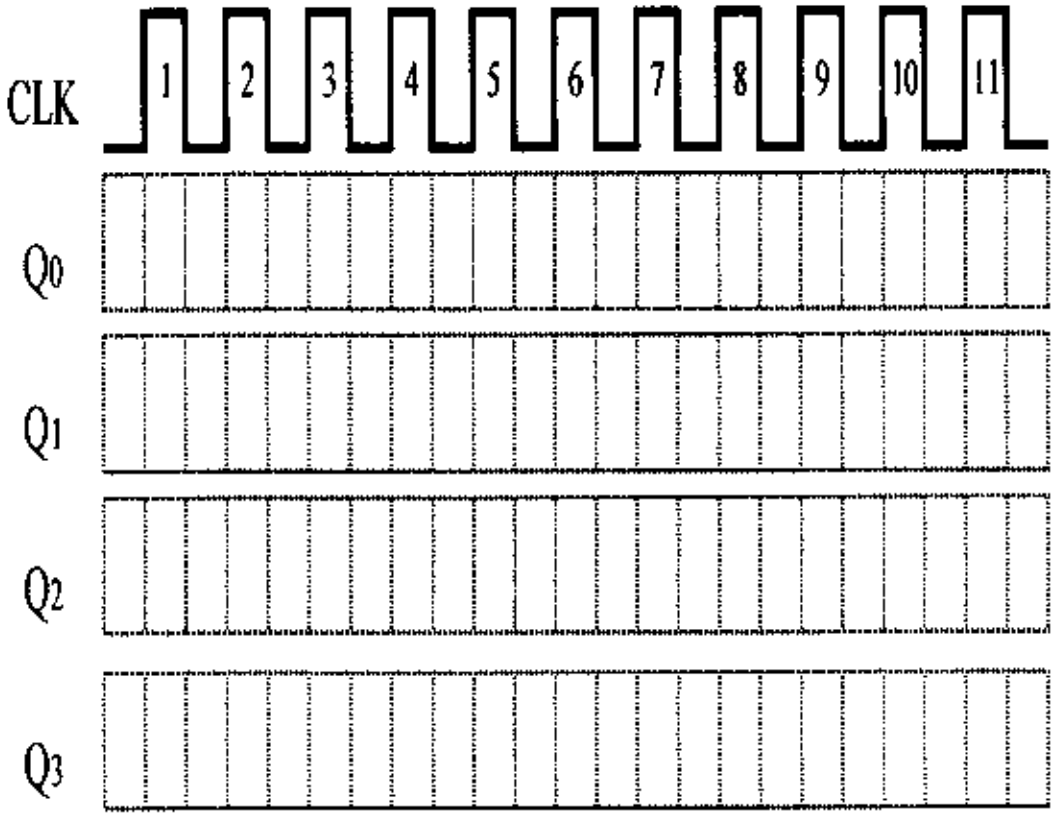


FIGURE Q2(a)

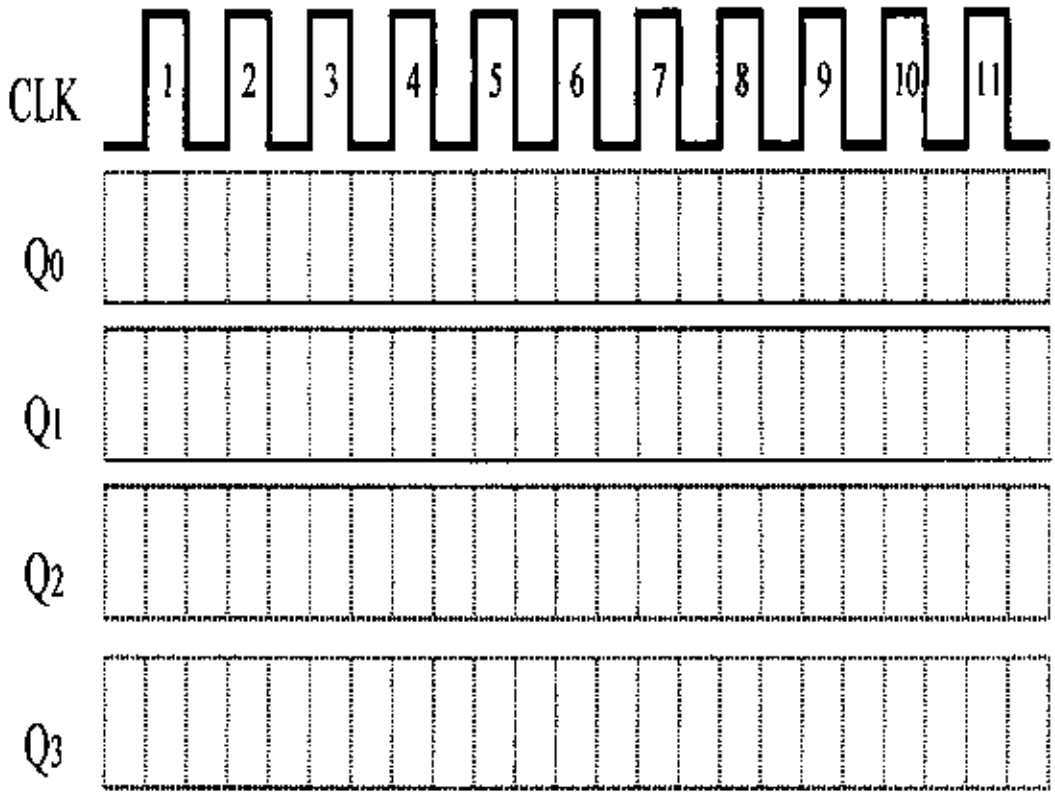
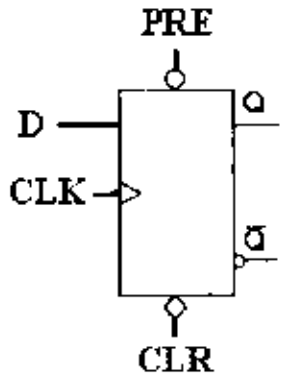


FIGURE Q2 (c)



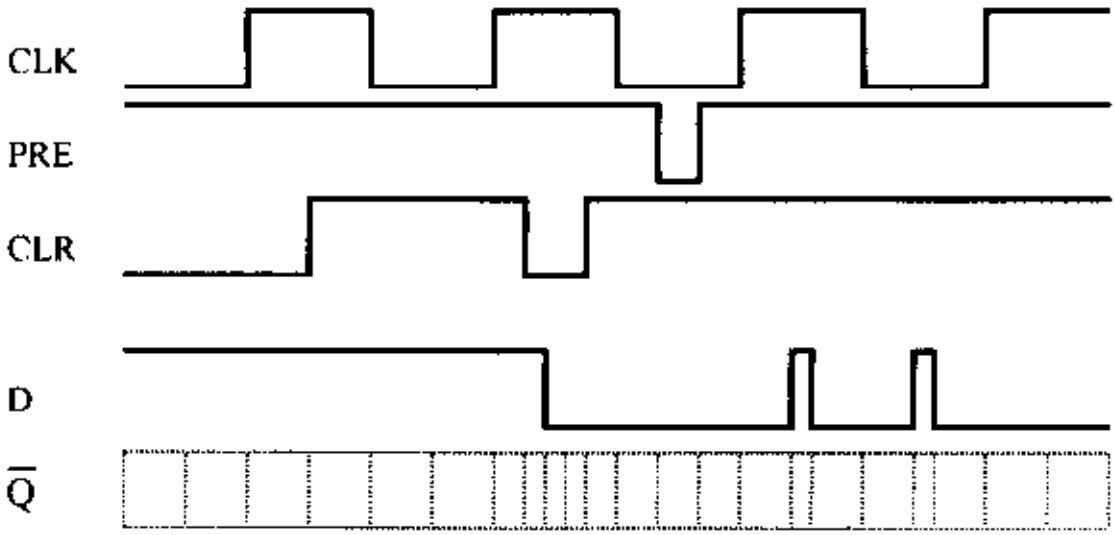


FIGURE Q3(d)

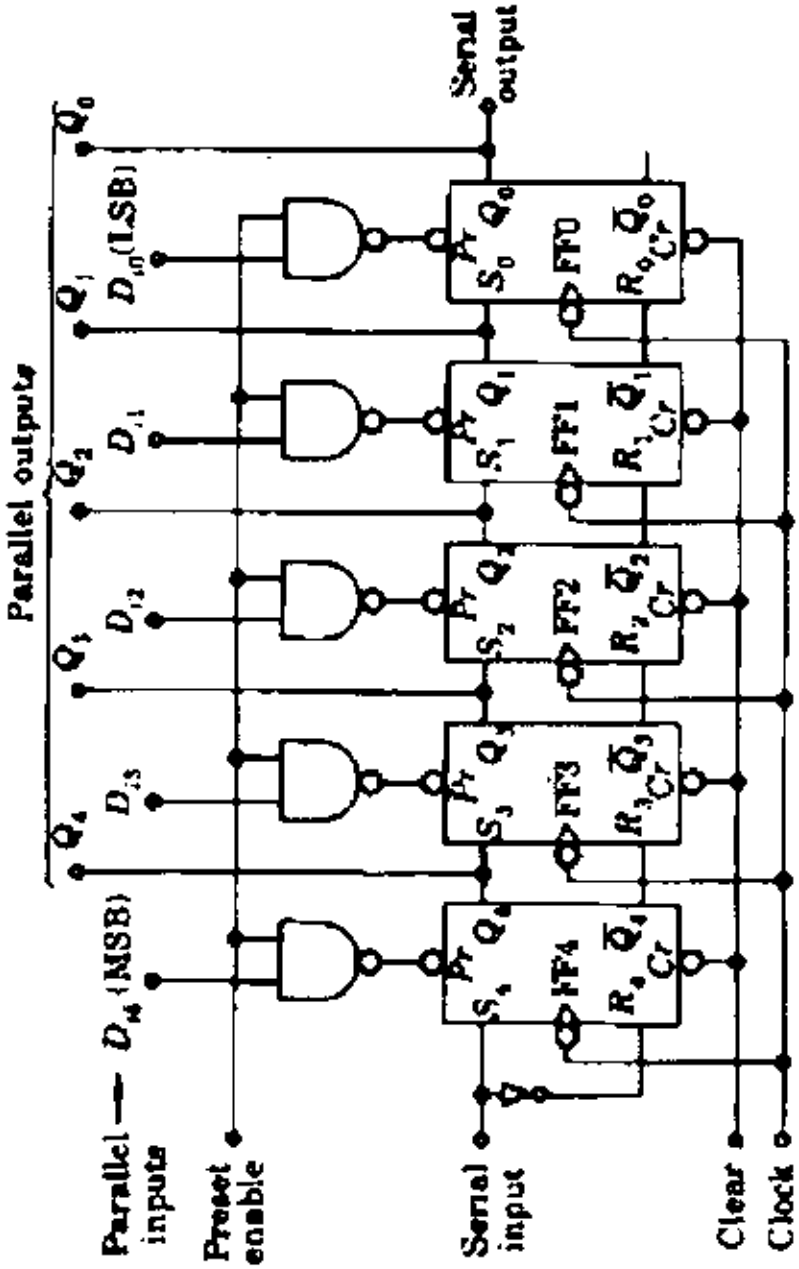

Serial output
Parallel outputs
Q_0
Q_1
Q_2
Q_3
Q_4
D_0 (LSB)
D_1
D_2
D_3
D_4 (MSB)
FF0
FF1
FF2
FF3
FF4
Parallel inputs
Preset enable
Serial input
Clear
Clock

FIGURE Q4 (b)(i)

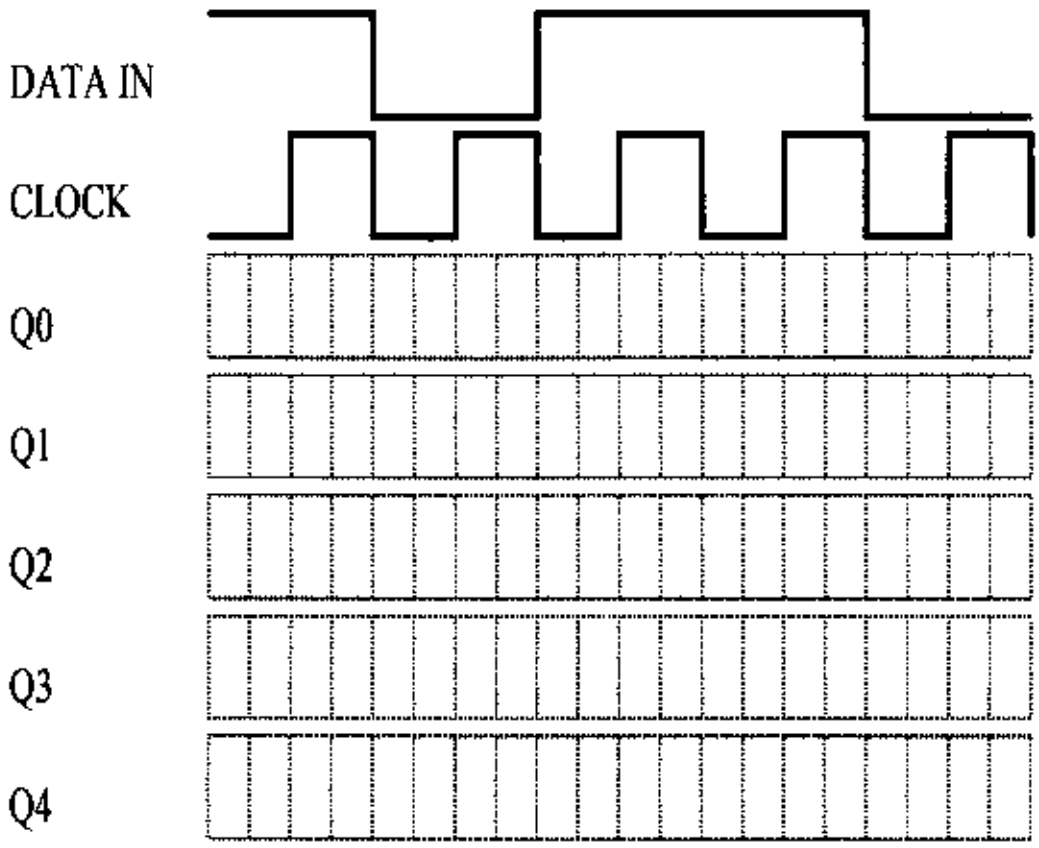
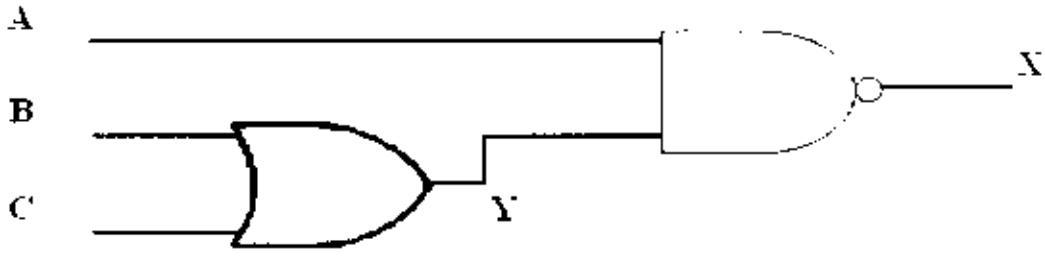


FIGURE Q4 (b)(ii)



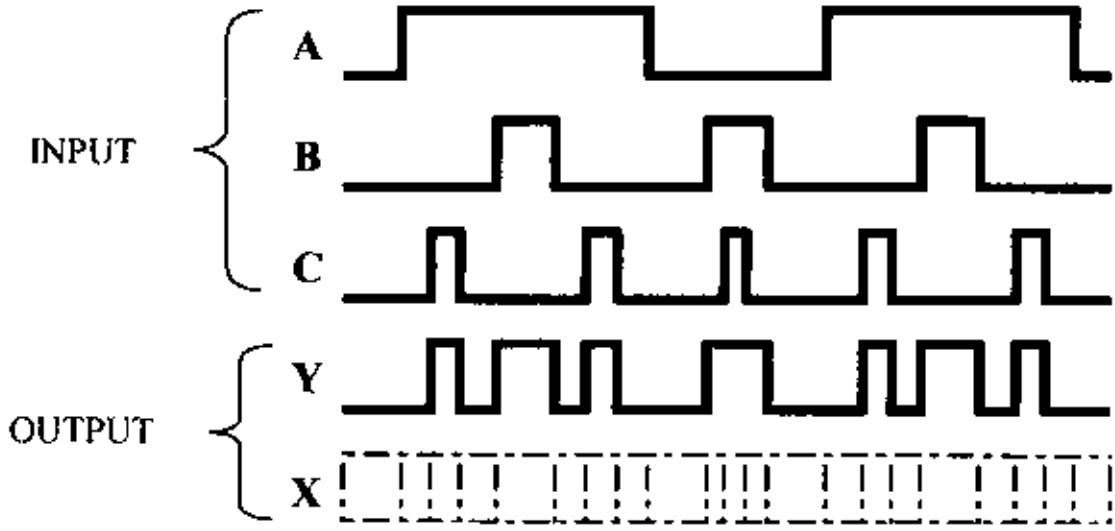


FIGURE Q5 (c)

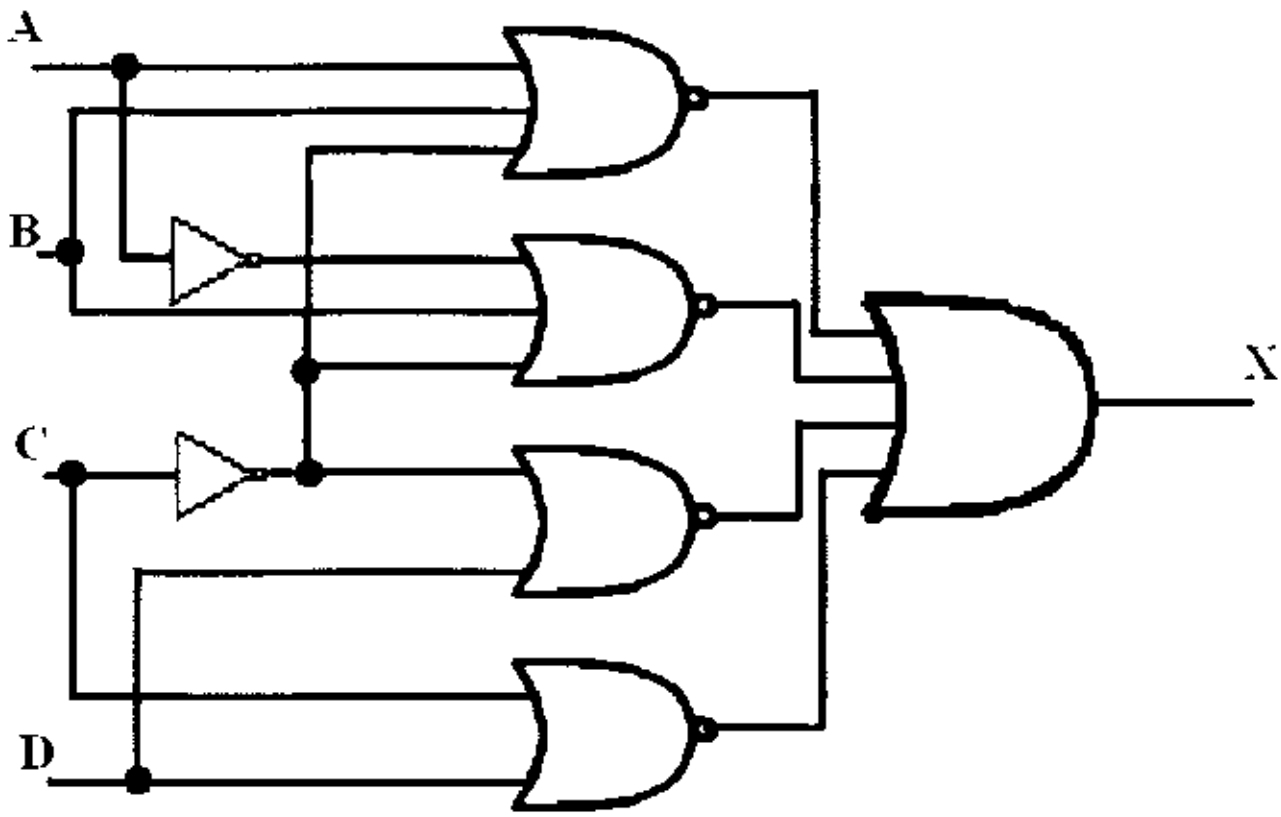


FIGURE Q6(a)

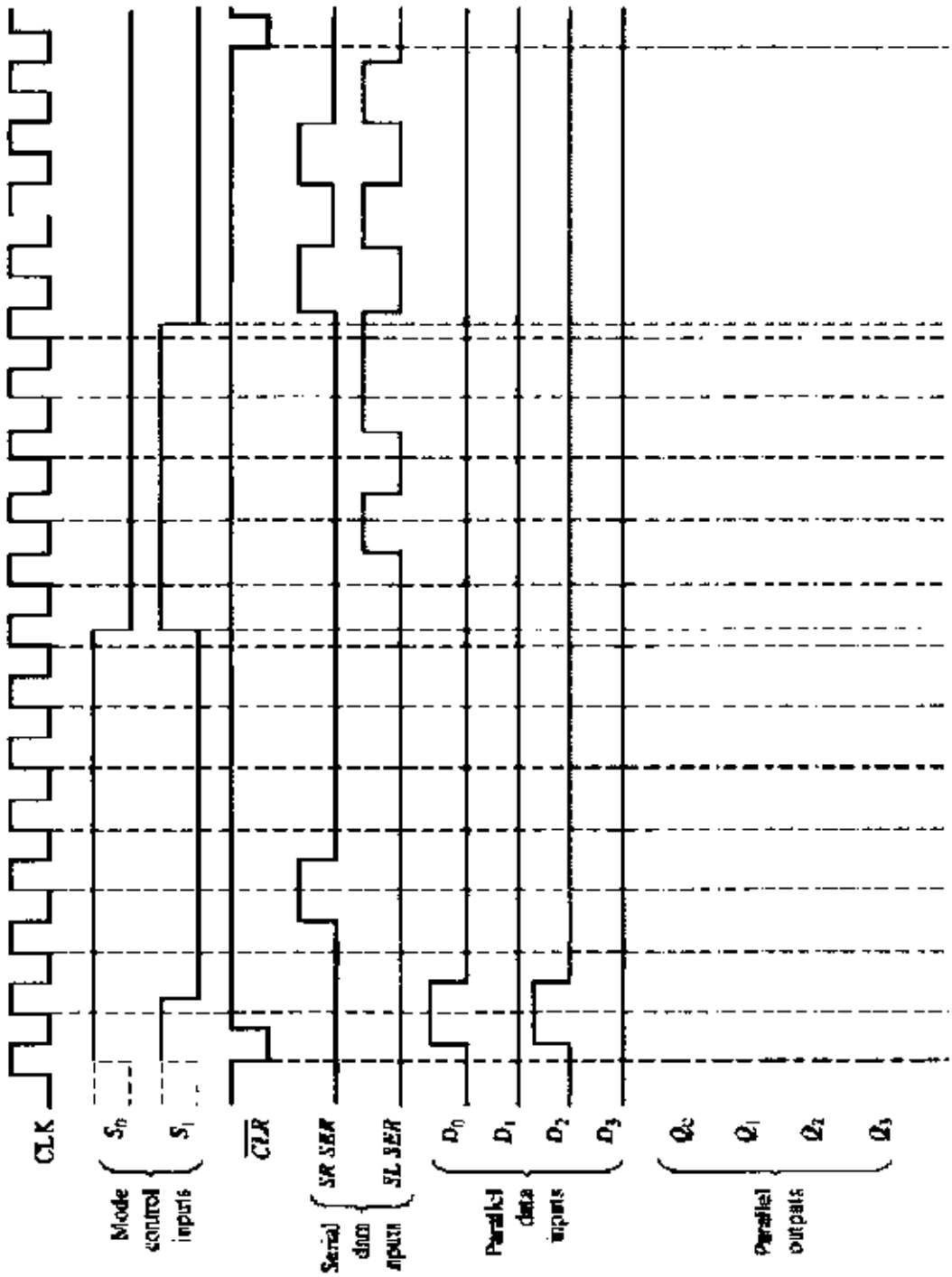

CLK
S_0
S_1
Mode control inputs
$\overline{CLR}$
SR SER
SL SER
Serial data inputs
D_0
D_1
D_2
D_3
Parallel data inputs
Q_0
Q_1
Q_2
Q_3
Parallel outputs

FIGURE Q8(a)

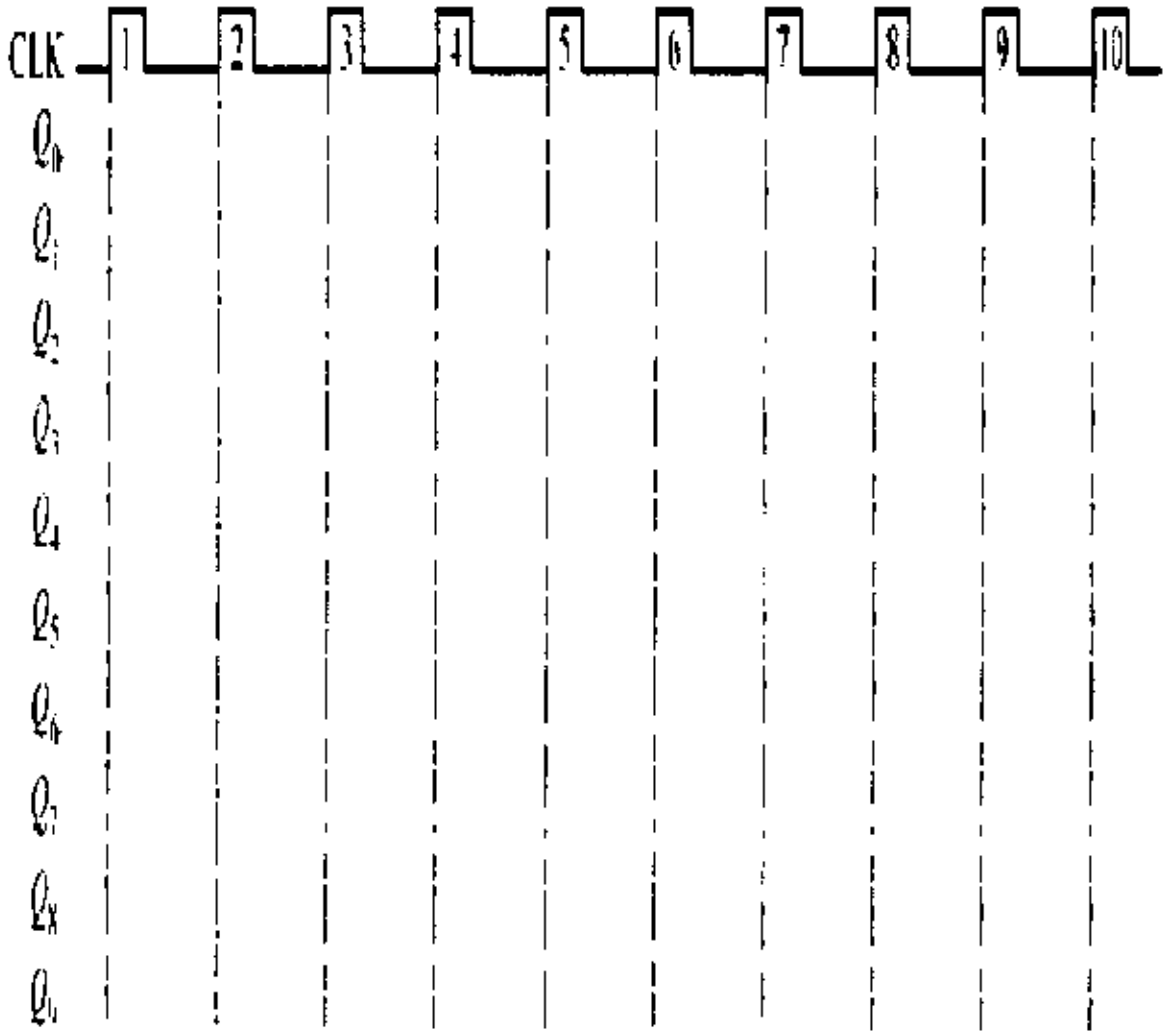


FIGURE Q8(b)

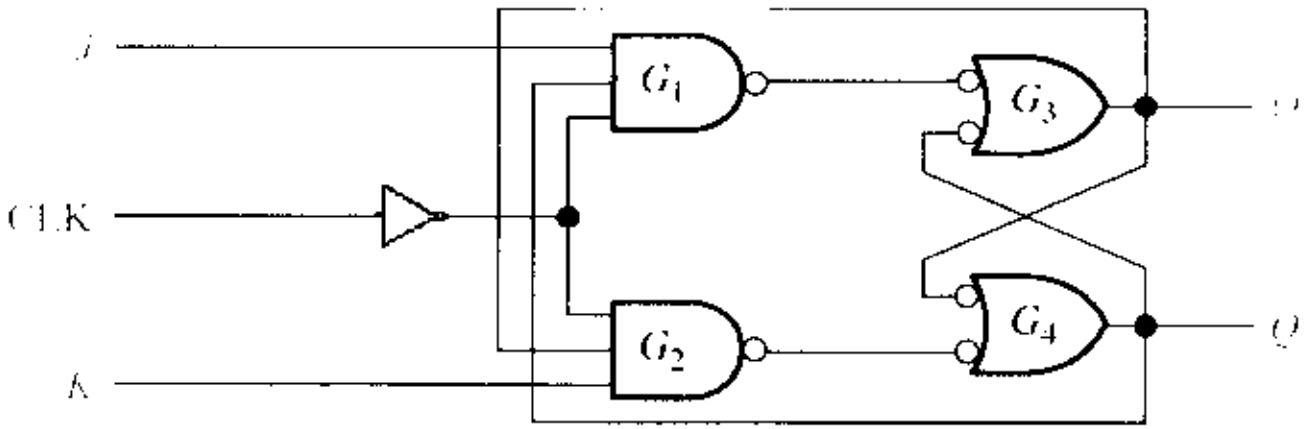


FIGURE Q10(a)(i)

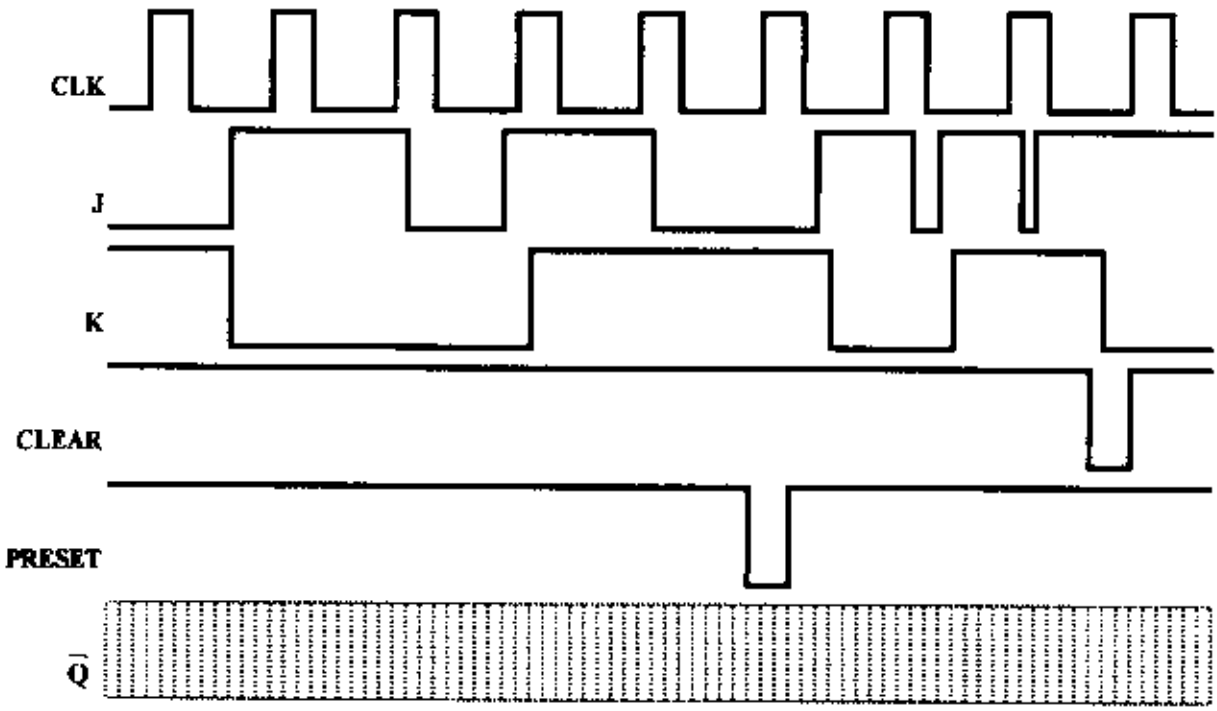


FIGURE Q10(a)(ii)

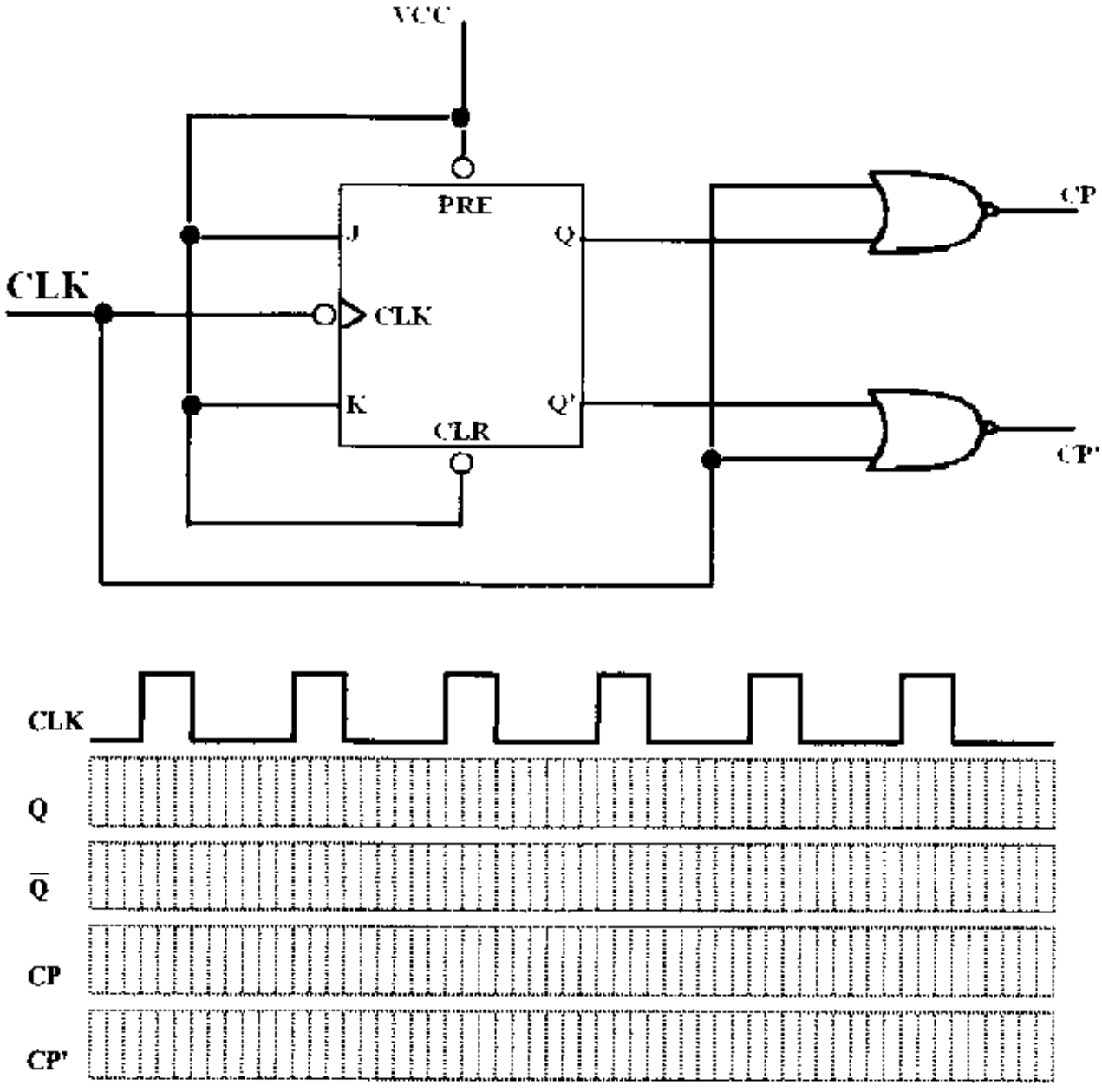


FIGURE Q10(b)