UNIVERSITI TUN HUSSEIN ONN MALAYSIA

FINAL EXAMINATION
SEMESTER I
SESSION 2011/2012

COURSE NAME	:	COMPUTER ARCHITECTURE
COURSE CODE	:	BIT 2033/BIT 20303
PROGRAMME	:	BACHELOR OF INFORMATION TECHNOLOGY
EXAMINATION DATE	:	JANUARY 2012
DURATION	:	3 HOURS
INSTRUCTION	:	ANSWER **ALL** QUESTIONS.

THIS QUESTION PAPER CONSISTS OF SEVEN (7) PAGES

PART A

Instruction: Answer **ALL** Questions

Q1 What is the most critical problem in performance balance?

A. Mismatch in the interface between processor and cache
B. Mismatch in the interface between processor and main memory
C. Mismatch in the interface between main memory and ALU
D. Mismatch in the interface between ALU and processor

Q2 Which of the following statements is **TRUE** about computer architecture and organization?

A. Architecture differs between different versions
B. Architecture changing with changing technology
C. All Intel x86 family share the same basic organization
D. Computer manufacturers offer a family of computer models with the same architecture but with difference in organization

Q3 A common measure of performance for a processor is the rate at which instructions are executed, expressed as _____.

A. cycles per instruction
B. millions of floating-points operations per second
C. millions of instructions per second
D. millions of operations per second

Q4 Who is accredited with developing the architecture of the modern computer?

A. John Mauchly
B. Charles Babbage
C. Jon von Neumann
D. John Eckert

Q5 An example of an embedded system is

A. A calculator
B. A machine tool
C. A CD-ROM
D. A water heating element

Q6 Which of the following is the **FALSE** statement of benchmark suites?

A. SPECjvm98 is to evaluate the performance of WWW server
B. SPECjbb2000 is to evaluate server-side Java-based electronic commerce applications
C. SPECmail2001 is to measure a system performance acting as a mail server
D. SPEC CPU2006 is to test processor intensive applications

Q7 What is the most important aspect of von Neumann model?

A. ALU and control unit are frequently referred to collectively as the CPU
B. Instructions and data are processed by the ALU
C. Input unit provides instructions and data to the system
D. Execution of a stored program

PART B

Instruction: Answer **ALL** Questions

Q8 Which of the following statements would be changes to the architecture (A) of a MIPS computer or to its organization (O)? State A or O to indicate your choice for each of the following statements.

(a) Increasing the CPU speed, while changing nothing else

(b) Increase a single chip processor to core processor

(c) Adding a third level cache

(3 marks)

Q9 Compute conversion for the following:

(a) Binary number 11110101_2 to hexadecimal

(2 marks)

(b) Convert this decimal number 155_{10} to binary number

(2 marks)

(c) Convert a decimal number 156_{10} to hexadecimal

(2 marks)

Q10 Define each of the following terms:

(a) Pipelining

(2 marks)

(b) Program Counter

(2 marks)

(c) Instruction

(2 marks)

Q11 Given the following statements:

A program has 25% division instructions. All non-division instructions take 4 cycles. All division instructions take 40 cycles. (Refer to formula at page 6)

(a) What is the CPI of this program on this processor?

(b) What percent of time is spent just doing division?

(c) What would the speedup be if we sped up division by 5x?

(d) What would the speedup be if division instructions were infinitely fast (zero cycles)?

(12 marks)

Q12 Illustrate instruction cycle diagram with interrupts.

(5 marks)

Q13 Explain **TWO (2)** approaches to deal with multiple interrupts.

(6 marks)

Q14 Give **TWO (2)** advantages and **TWO (2)** disadvantages of multiplexed bus types.

(4 marks)

Q15 Briefly state the task for the following buses:

(a) Control bus

(2 marks)

(b) Address bus

(2 marks)

(d) Data bus

(2 marks)

Q16 Explain the operation of the bus system if a module wishes to request data from another module.

(5 marks)

PART C

Instruction: Answer **ALL** Questions

Q17 Discuss **FIVE (5)** important elements to be considered in order to produce a high performance computer.

(10 marks)

Q18 Design a **2-bit calculator** using logical gates. Below are samples of 2-bit calculation.

$01_2 + 01_2 = 10_2$
$10_2 + 00_2 = 10_2$
$11_2 + 11_2 = 110_2$

(10 marks)

Q19 Discuss **FIVE (5)** important elements to be considered in order to design a high speed bus.

(10 marks)

Q20 Elaborate on **THREE (3)** techniques that can be used to enhance the performance of a **CPU**.

(10 marks)

FORMULA

$$CPI = \frac{\sum_{i=1}^{n}(CPI_i \times I_i)}{I_c}$$

$$MIPS = \frac{I_c}{T \times 10^6} = \frac{f}{CPI \times 10^6}$$

$$r_i = \frac{Tref_i}{Tsut_i}$$

$$r_G = \left(\prod_{i=1}^{n} r_i \right)^{1/n}$$

$$r_i = \frac{N \times Tref_i}{Tsut_i}$$

$$Speedup = \frac{\text{time to execute program on a single processor}}{\text{time to execute program on } N \text{ parallel processors}} = \frac{T(1-f)+Tf}{T(1-f)+\frac{Tf}{N}} = \frac{1}{(1-f)+\frac{f}{N}}$$

$$Speedup = \frac{1}{(1-f)+\frac{f}{SU_f}}$$