UNIVERSITI TUN HUSSEIN ONN MALAYSIA

FINAL EXAMINATION
SEMESTER II
SESSION 2012/2013

COURSE NAME	:	COMPUTER ARCHITECTURE
COURSE CODE	:	BIT 20303
PROGRAMME	:	1 BIT
EXAMINATION DATE	:	JUNE 2013
DURATION	:	3 HOURS
INSTRUCTION	:	ANSWER **ALL** QUESTIONS

THIS QUESTION PAPER CONSISTS OF **FOUR (4)** PAGES

Q1 (a) What is CPU? What are its primary components?

(5 marks)

(b) What are registers? Give **ONE (1)** example of register and briefly explain its functions.

(5 marks)

(c) Describe the function of main memory.

(2 marks)

(d) State **THREE (3)** differences between register and main memory.

(3 marks)

(e) Discuss **TWO (2)** methods of data access to a memory location.

(5 marks)

Q2 (a) Consider the following scenario:

On the IAS computer system, the process of an instruction cycle comprises of fetch and executes cycle. Based on **FIGURE Q2 (a)**, assume the operation code 1 stored at address 301 is a LOAD operation.

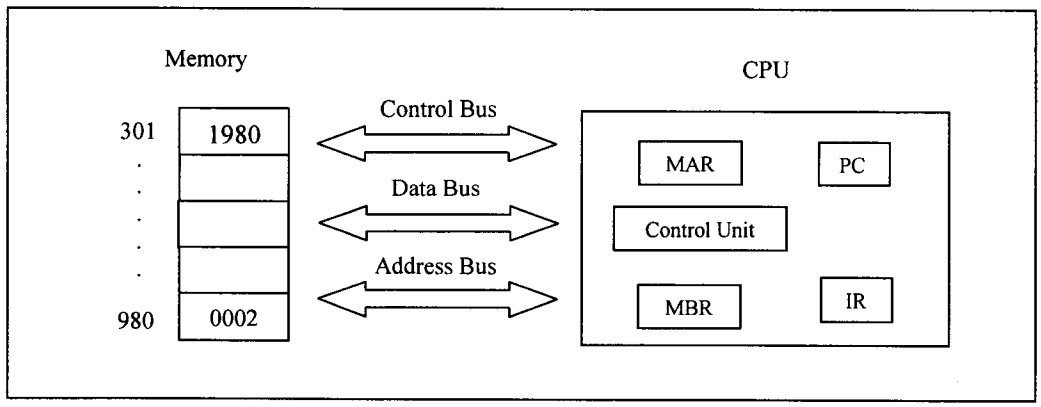

FIGURE Q2 (a)

Describe how the load operation works. Your answer must include the data movement to/from these registers - PC, MAR, MBR, IR, address bus, data bus and control bus.

(10 marks)

(b) An interrupt occurs exactly at the instance of a processor fetches an instruction. Describe how the processor service this interrupt by assuming only a single interrupt occurs.

(10 marks)

Q3 (a) Compute the sums of the following pairs of unsigned integers:

(i) 1100 1100 + 0011 0011
(ii) 0111 1111 + 0000 0001

(4 marks)

(b) Compute the product of the following pairs of unsigned integers. Generate the full 8-bit result.

(i) 1001 × 0110
(ii) 1111 × 1111

(6 marks)

(c) Convert the following quantities to IEEE single point-precision floating-point:

(i) 1011 1101 0100 0000 0000 0000 0000 0000
(ii) 0101 0101 0110 0000 0000 0000 0000 0000

(10 marks)

Q4 (a) Some memory requires condition code.

(i) Which register requires condition codes?

(2 marks)

(ii) Explain any **FOUR (4)** condition codes with appropriate example for each.

(8 marks)

(b) A pipeline processor works in **FOUR (4)** stages: fetch instruction (FI), decode instruction and calculate address (DI), fetch operand (FO) and execute instruction (EX). Complete the timing diagram for this instruction pipeline operation as shown in **FIGURE Q4 (b)** for a sequence of seven instructions in which the third instruction is a branch that is taken and in which there are no data dependencies.

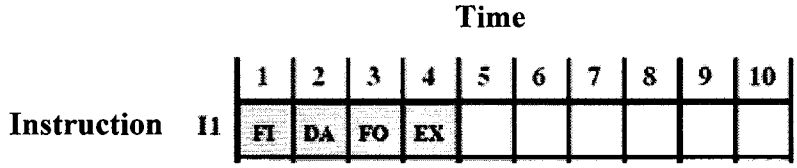

FIGURE Q4 (b)

(10 marks)

Q5 (a) Given a C statement as shown in **FIGURE Q5 (a)**. Convert this C statement into a full program in assembly language based on 8086 instruction set. Use AX and BX register to store the variable's value.

```
int a = 26;
int b = 5;
int c = a + b;

printf("%d",c);
```

FIGURE Q5 (a)

(10 marks)

(b) Write a complete program in assembly language based on 8086 instruction set to display the letter 'a' on the screen.

(10 marks)

-END OF QUESTION -