Universiti Tun Hussein Onn Malaysia

UNIVERSITI TUN HUSSEIN ONN MALAYSIA

FINAL EXAMINATION
SEMESTER II
SESSION 2016/2017

COURSE NAME	:	COMPUTER ARCHITECTURE
COURSE CODE	:	BIC 10503
PROGRAMME CODE	:	1 BIS / BIM / BIP / BIW
EXAMINATION DATE	:	JUNE 2017
DURATION	:	2 HOURS 30 MINUTES
INSTRUCTION	:	ANSWER **ALL** QUESTIONS

THIS QUESTION PAPER CONSISTS OF **SIX (6)** PAGES

SECTION A
Instruction: Determine whether each of these statements are TRUE or FALSE.

Q1 Microarchitecture is the embedded programming language of the central processing unit.

Q2 ENIAC had to be programmed manually by setting switches, plugging and unplugging cables.

Q3 A particular computer architecture may span many years and encompass a number of different computer models while its organization changing with changing technology.

Q4 All computer functions must be able to perform data storage, data movement and data processing.

Q5 Arithmetic and logic unit (ALU) performs the computer's data processing function.

Q6 L1 and L2 are levels of cache memory in a computer where the computer processor can find the data it needs for its next operation in secondary memory.

Q7 The speed of a computer is measured by the pulse frequency generated by the clock, measured in Hertz (Hz) unit.

Q8 During execute cycle, processor interprets instruction and performs required actions.

Q9 Direct memory access (DMA) can be used for data exchanges between I/O devices and memory, and no interrupt is needed.

Q10 Bus width determines the source or destination of data.

(10 marks)

SECTION B
Instruction: Choose the BEST answer for each of the following questions.

Q11 The disadvantage of Dynamic Random Access Memory (DRAM) over Static Random Access Memory (SRAM) is _____.

A. lower data storage capacity
B. higher heat descipation
C. the cells are not static
D. all of the above

Q12 The effectiveness of the cache memory is based on the property of _____.

A. locality of reference
B. memory localization
C. memory size
D. none of the above

Q13 The instructions which copy information from one location to another either in the processor's internal register set or in the external main memory are called _____.

A. data transfer instruction
B. program control instructions
C. input-output instructions
D. logical instructions

Q14 _____ is the bus master in centralized arbitration.

A. Processor
B. DMA Controller
C. Device
D. A and B

Q15 The average time required to reach a storage location in memory and obtain its contents is called _____.

A. latency time
B. access time
C. input time
D. response time

Q16 _____ register keeps tracks of the instructions stored in program stored in memory.

A. Address Register (AR)
B. Index Register (IX)
C. Program Counter (PC)
D. Accumulator (AC)

Q17 The disadvantage of the Erasable Programmable Read Only Memory (EPROM) chip is _____.

A. the high cost factor
B. the low efficiency
C. the low speed operation
D. the need to remove chip physically to reprogram it

Q18 $2FAOC_{16}$ is equivalent to _____.

A. $195\ 084_{10}$
B. $001011111010\ 0000\ 1100_2$
C. both A and B
D. none of the above

Q19 Which of the following operations that is not performed by a CPU?

A. Logic operation
B. Arithmetic operation
C. Data transfer
D. Control

Q20 The signal sent to the device from the processor after receiving an interrupt is _____.

A. interrupt acknowledge
B. return signal
C. service signal
D. permission signal

(10 marks)

SECTION C

Q21 (a) Calculate the Hamming code word for the message `10011011011`.

(5 marks)

(b) Invert one bit of Hamming code word in **Q21(a)** at the leftmost to represent 1-bit error and show the bit verification.

(5 marks)

Q22 (a) Give **FOUR (4)** techniques for I/O operations to read data from a device to memory?

(4 marks)

(b) State **THREE (3)** differences between memory-mapped I/O and isolated I/O?

(6 marks)

Q23 (a) Simplify the following Boolean expressions using Karnaugh Map and draw the logic circuits.

$f = \bar{w}x\bar{y}z + \bar{w}xyz + \bar{w}xy\bar{z} + wx\bar{y}z + wxyz + wxy\bar{z} + w\bar{x}\bar{y}z + w\bar{x}yz$

(10 marks)

(b) Give **TWO (2)** types of locations that can hold source and destination operands.

(2 marks)

(c) Describe **FOUR (4)** elements of an instruction.

(8 marks)

Q24 (a) Describe the **SIX** (6) stages of instruction pipeline.

(12 marks)

(b) Describe the basic task of a control unit.

(2 marks)

(c) Identify the **FOUR (4)** inputs and **TWO (2)** outputs of a control unit in Figure **Q24(c)**.

(6 marks)

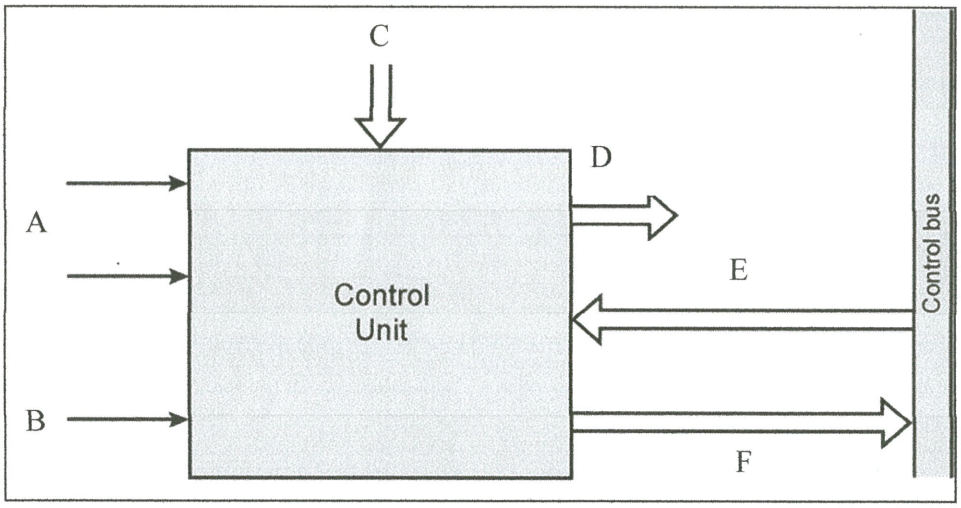

FIGURE Q24(c)

- END OF QUESTION -