Universiti Tun Hussein Onn Malaysia

UNIVERSITI TUN HUSSEIN ONN MALAYSIA

FINAL EXAMINATION
SEMESTER II
SESSION 2016/2017

COURSE NAME	:	COMPUTER ARCHITECTURE
COURSE CODE	:	BIT 20303
PROGRAMME CODE	:	BIT
EXAMINATION DATE	:	JUNE 2017
DURATION	:	3 HOURS
INSTRUCTION	:	ANSWER **ALL** QUESTIONS

THIS QUESTION PAPER CONSISTS OF **FIVE (5)** PAGES

Q1 (a) A disk is divided into tracks and sectors. Give a brief description of track and sector by using a labeled diagram.

(6 marks)

(b) Reddundant Array of Independent Disk (RAID) is a computer data storage schemes that can divide and replicate data among multiple physical drives. Identify **TWO (2)** characteristics shared by all RAID levels.

(4 marks)

Q2 (a) Perform the following 8 bit arithmetic operation in two's-complement notation. Show your calculation:

(i) $18_{10} - 20_{10}$

(2 marks)

(ii) $-12_{10} + 30_{10}$

(2 marks)

(b) Compute the product for each of the following pairs of unsigned integer. Generate the full 8-bit result.

(i) 1001×0110

(3 marks)

(ii) 1111×1111

(3 marks)

Q3 (a) The indirect cycle is an additional stage for instruction cycle which requires additional memory access.

(i) Outline the indirect cycle data flow process involved using any related diagram.

(4 marks)

(ii) Based on **Q3(a)(i),** describe your answer in terms of what data is placed on Program Counter (PC) Memory Address Register (MAR), Memory Buffer Register (MBR), Instruction Register (IR), address bus, data bus and control bus during indirect cycles.

(4 marks)

	1	2	3	4	5	6	7	8	9	10
I1	FI	DA	FO	EX						

Figure Q3(b)

(b) **Figure Q3(b)** shows four (4) stages of pipeline processor. Pipelining processor containing fetch instruction (FI), decode instruction and calculate address (DI), fetch operand (FO) and execute instruction (EX). Analyze the processes involved and complete the timing diagram for this instruction pipeline operation for a sequence of seven instructions, in which the third instruction is a branch that is taken and in which there are no data dependencies.

(10 marks)

(c) The registers in the processor perform **TWO (2)** roles. Describe each role.

(4 marks)

Q4 Input/Output (I/O) module is not simply a set of mechanical connectors that wire a device into the system bus.

(a) Examine **TWO (2)** reasons why I/O devices do not connect directly to the system bus.

(4 marks)

(b) External devices can be broadly classified into **THREE (3)** categories. Describe each category and support your answer with an example.

(6 marks)

(c) Interrupt I/O is more efficient than simple programmed I/O .

(i) Identify the weakness in programmed I/O and interrupt I/O that requires the existence of Direct Memory Access (DMA).

(2 marks)

(ii) How DMA overcome those weaknesses based on **Q4(c)(i)**.

(4 marks)

(d) Differentiate between parallel interface and serial interface.

(4 marks)

Q5 **Figure Q5** shows a general model of the control unit showing all of it inputs and outputs.

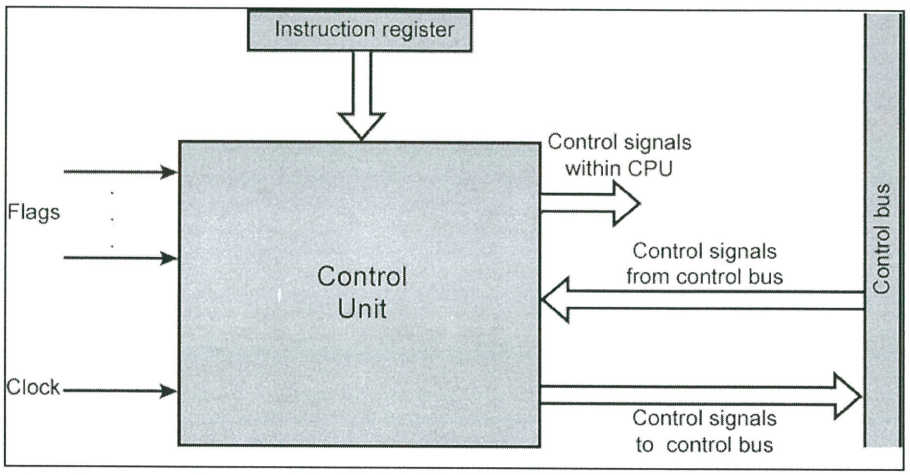

Figure Q5

(a) Classify all the inputs and outputs and explain each of them.

(6 marks)

(b) Explain how Control Unit operates.

(6 marks)

Q6 A Direct Mapped Cache provides a specific cache location for any address in main memory. Determine the Tag, Line and Word values for a Direct Mapped Cache of the given main memory addresses. Show your work. Your answer should be in hexadecimal.

(a) 111111

(5 marks)

(b) BBBBBB

(5 marks)

Q7 (a) State **FOUR (4)** advantages of a shared L2 cache among cores compared to separate dedicated L2 caches for each core.

(8 marks)

(b) Propose **FOUR (4)** methods to improve the Microprocessor speed.
(8 marks)

- END OF QUESTION -