UNIVERSITI TUN HUSSEIN ONN MALAYSIA

PEPERIKSAAN AKHIR
SEMESTER II
SESI 2008/09

NAMA MATA PELAJARAN	:	ELEKTRONIK DIGIT
KOD MATA PELAJARAN	:	BEE 2233
KURSUS	:	2 BEE
TARIKH PEPERIKSAAN	:	APRIL 2009
JANGKA MASA	:	2 JAM 30 MINIT
ARAHAN	:	JAWAB **EMPAT (4)** SOALAN SAHAJA DARIPADA ENAM (6) SOALAN.

KERTAS SOALAN INI MENGANDUNGI 9 MUKA SURAT

SOALAN DALAM BAHASA INGGERIS

Q1 (a) Simplify the function

$$F = \bar{a}\cdot\bar{b}\cdot\bar{c}\cdot\bar{d} + \bar{a}\cdot b\cdot\bar{c}\cdot\bar{d} + a\cdot\bar{b}\cdot\bar{c} - a\cdot\bar{b}\cdot\bar{d}$$

With don't care states $\bar{a}\cdot\bar{b}\cdot\bar{c}\cdot d$ and $\bar{a}\cdot\bar{b}\cdot c\cdot\bar{d}$ to give expression in the following form:

(i) sum of products; (5 marks)

(ii) standard sum of product. (5 marks)

(b) An assembly line has 3 active-HIGH failsafe sensors and 1 emergency shutdown active-LOW switch. The line should keep moving unless any of the following conditions arise:

- If the emergency switch is pressed.
- If sensor 1 and sensor 2 are activated at the same time.
- If sensor 2 and sensor 3 are activated at the same time.
- If all three sensors are activated at the same time.

To stop the assembly line, signal HIGH must be generated at the output, Z.

(i) Derive the truth table for this system. (10 marks)

(ii) Obtain the simplest Boolean expression for Z. (5 marks)

Q2 (a) How do don't care arise in practice and how may they be exploited? Are there any pitfalls in using them? Illustrate your answer with example. (5 marks)

(b) Design a 2-bit multiplier for unsigned integers which takes input $x_1\ x_0$ representing the unsigned integer X, $y_1\ y_0$ representing the unsigned integer Y , and produces the output $Z_3Z_2Z_1Z_0$ representing the unsigned integer Z. Start from truth table and obtain the simplest Boolean expression using Karnaugh map technique. Finally, draw the circuit. (13 marks)

(c) Figure Q2(c) shows logic symbol of two 2-bit binary multiplier and a 4-bit parallel binary adder. Illustrate how the 2-bit multiplier can be be cascaded (with adders) to implement a four-bit multiplier? (7 marks)

Q3 (a) Illustrate and prove how two half adder can be combined to form a full adder? (8 marks)

(b) Explain with example, what is an 'overflow' condition in a signed arithmetic operation. (5 marks)

(c) Assume that the binary adder / subtractor shown in the figure Q3(c) is to handle signed binary numbers in which x_{n-1} and y_{n-1} are the sign bits. Two methods can be used for the detection of an overflow condition, one based on the sign bits of the operands and the other based on the carry into and from the sign digit position during addition.

(i) Determine the additional logic needed if an overflow condition is to be detected based on the sign bits of the operands. (6 marks)

(ii) Determine the additional logic needed if an overflow condition is to be detected based on the carry into and from the sign digit position during addition. (6 marks)

Q4 (a) Simplify the function

$$F = (\bar{a} + \bar{b} + \bar{c}) \cdot (b + d)$$ (2 marks)

(b) Implement with a 2-input logic gates the function in Q4(a) using only

(i) NOR gates (3 marks)

(ii) NAND gates (3 marks)

(c) An electronic die may be constructed from seven LEDs laid out in the pattern shown in Figure Q4(c)(i). The LEDs are to be driven by binary input b2, b1 and b0.

(i) Build the truth table for this electronics die if its required to display number such as shown in figure Q4(c)(i) (10 marks)

(ii) Illustrate the implementation of this circuit using IC74138 logic symbol and additional logic gates. You may refer to Figure Q4(c)(ii) for the internal circuitary and logic symbol (7 marks)

Q5 (a) State De Morgan's theorems. (2 marks)

(b) Describe the operation of the following MSI logic circuit

(i) Multiplexer (3 marks)

(ii) Encoder (3 marks)

(c) Eight sensors each feed eight bits of information to a circuit which processes the information. It is decided that instead of using 64 signal lines, the data will be multiplexed onto eight data lines with three address lines used to indicate the sensor using the data lines. In fact, the sensors will be continually cycled through in order.

(i) A three-bit counter is required to cycle through the values for the address lines. Design it using JK flip-flop. You may assume the availability of a clock signal. (6 marks)

(ii) An 8:1 multiplexer has eight data inputs, three control inputs and an output. The value of the control inputs determines the data input which is selected as the output. Design an 8:1 multiplexer. (6 marks)

(iii) Show how these components would be used to build the required system. (5 marks)

Q6 (a) A 4-bit shift register constructed from edge-triggered D-type flip flops is shown in Figure Q6(a). If, on successive rising edges of the clock signal CLK, the input takes on the values 1, 0, 1, 0, 1, 1, 1, 0, what are the contents of the shift register after each edge of the clock? You may assume that the register contains all zeroes initially. (3 marks)

(b) The shift register in Q6(a) is require to detect '1011' bit pattern from the serial data feed into the input pin. Design and illustrate how a combinational logic circuit can be added to achieve this. This combinational logic circuit will produce an output HIGH (1) when the pattern is detected. (7 marks)

(c) Figure Q6(c) shows a state transition diagram for an infinite state machine with control input, Y. Design the circuit using JK flip-flop. (15 marks)

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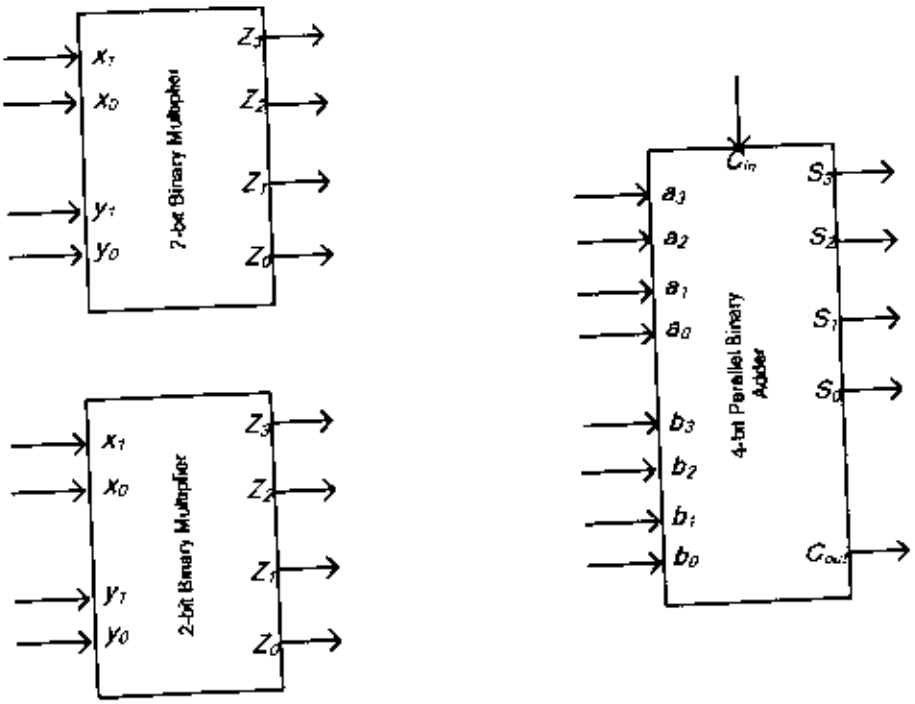

FIGURE Q2(c)

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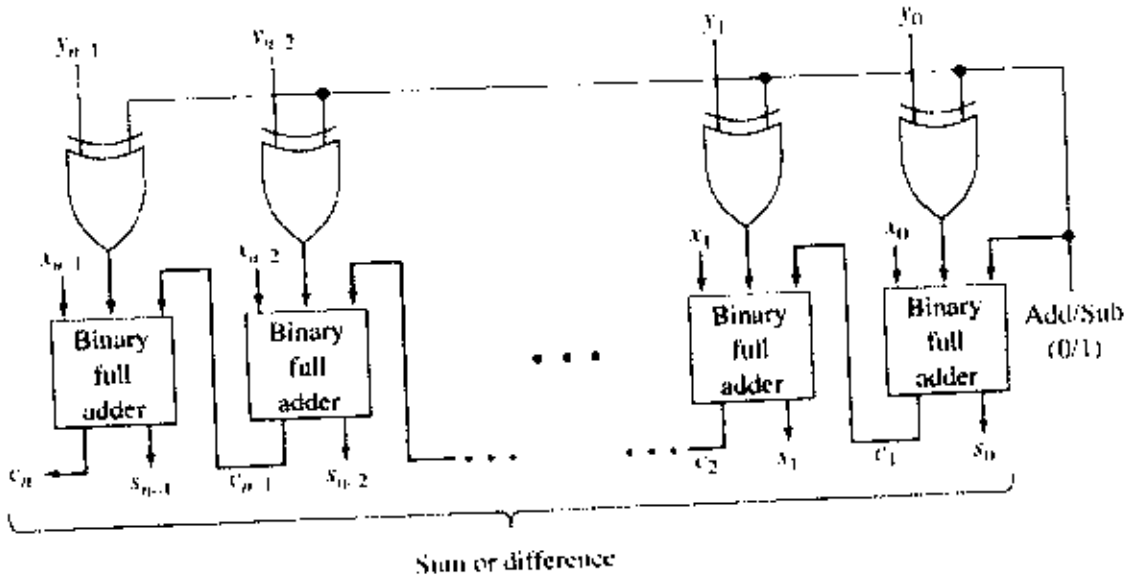

FIGURE Q3(c)

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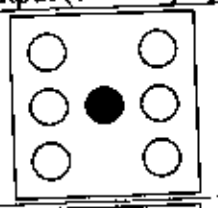
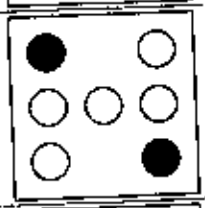
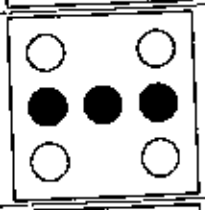
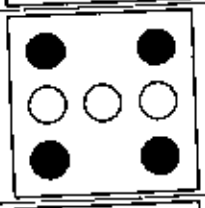
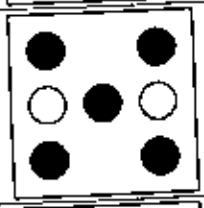
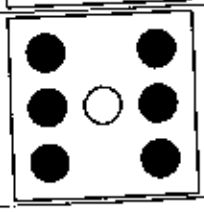
Input (decimal)	Output (dice display)
1	
2	
3	
4	
5	
6	

FIGURE Q4(c)(i)

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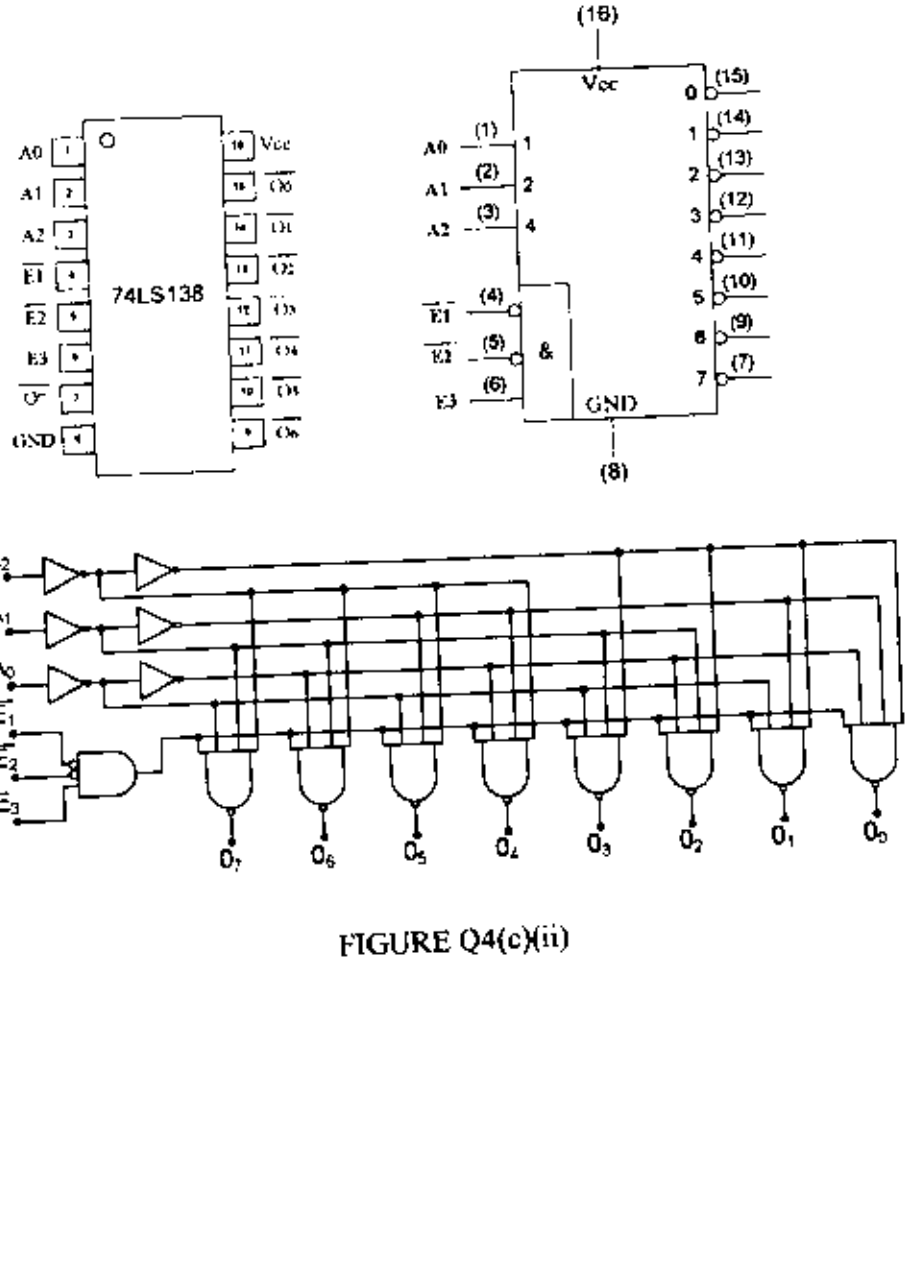

FIGURE Q4(c)(ii)

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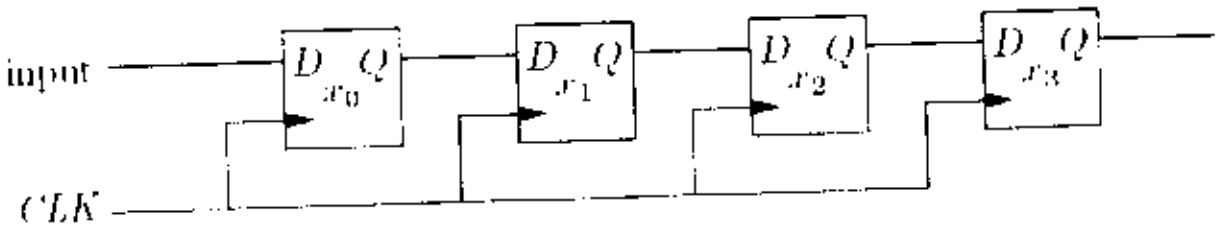

FIGURE Q6(a)

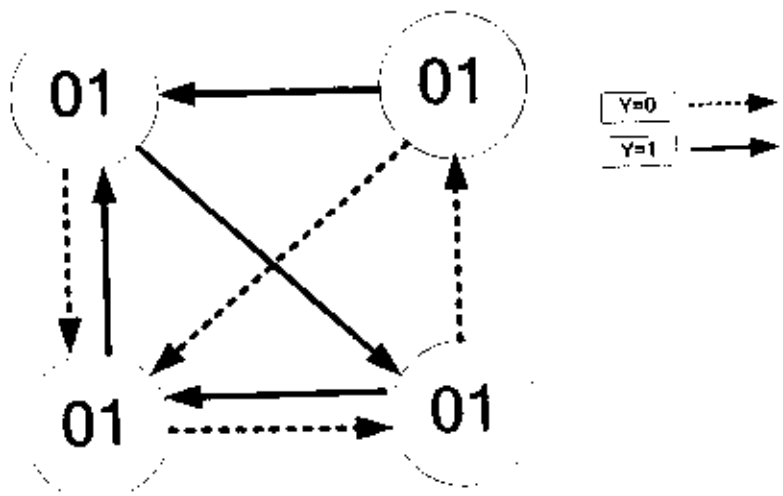

FIGURE Q6(c)