UNIVERSITI TUN HUSSEIN ONN MALAYSIA

FINAL EXAMINATION
SEMESTER II
SESSION 2009/2010

COURSE NAME	: LOGIC SYSTEM
COURSE CODE	: DEE 2233
PROGRAMME	: 2 DET / DEE / DEX
EXAMINATION DATE	: APRIL/MAY 2010
DURATION	: 3 HOURS
INSTRUCTION	: **PART A** : ANSWER **ALL** QUESTIONS
	PART B : ANSWER **THREE (3)** QUESTION ONLY

THIS PAPER CONSISTS OF SIXTEEN (16) PAGES

PART A

Q1 (a) Draw an active LOW input R-S latch logic diagram and build its truth table.

(3 marks)

(b) Modify the logic diagram that you have drawn in part Q1(a) if a signal ENABLE is applied.

(2 marks)

(c) Sketch the Q output waveform for the logic diagram at in part Q1(b), when the input waveforms EN, S and R as shown in Figure **Q1**(c) are applied.

(3 marks)

Q2 (a) Draw the logic symbol for a negative edge-triggered S-R flip-flop and J-K flip-flop.

(2 marks)

(b) What is the difference between a latch and a flip-flop? Give **ONE (1)** reason by sketching using logic symbol.

(2 marks)

(c) Show how a Positive Edge Triggered D Flip-Flop can be implemented using an S-R flip-flop and inverter.

(2 marks)

(d) The input waveforms in Figure **Q2**(d) are applied to CLK, D, PRE and CLR as indicated. Determine and draw the output waveform.

(2 marks)

Q3 (a) Draw a logic diagram for three-bit asynchronous binary counter using positive edge-triggered J-K flip-flop and sketch the complete timing diagram using CLK input in Figure **Q3**(a).

(3 marks)

(b) Determine the maximum clock frequency at which the counter can be operated for a 3-bit asynchronous binary counter if each negative edge-triggered flip-flop has a propagation delay for 15 ns.

(2 marks)

(c) Draw a logic diagram for three-bit synchronous binary counter using negative edge-triggered flip-flop and sketch the complete timing diagram using CLK input in Figure **Q3**(c).

(3 marks)

Q4 (a) Show how a NOR gate can be implemented by using only **FOUR (4)** NAND gates.
(2.5 marks)

(b) Show how an AND gate can be implemented by using only **THREE (3)** NOR gates.
(2.5 marks)

(c) Sketch the output waveform, X for the circuit shown in Figure **Q4**(c), by referring to the given input waveforms A, B and C and output waveform Y.
(3 marks)

Q5 (a) State **FOUR (4)** possible mode of register operation and draw **TWO (2)** logic diagram from the possible mode of register operation.
(4 marks)

(b) Determine the state of the shift register of Figure **Q5**(b) *a*fter each clock pulse for the given RIGHT/LEFT' control input waveform in Figure **Q5**(b). Assume $Q_0 = 1$, $Q_1 = 1$. $Q_2 = 0$, $Q_3 = 1$ and that the serial data-input line is LOW.
(4 marks)

PART B (Show all your steps)

Q6 (a) Using the IC 555 Timer and RC component, draw the complete schematic diagram for Monostable (One-Shot) operation and Astable operation.

(6 marks)

(b) Determine **TIME WIDTH** (t_w) for monostable (One-Shot) if given **ENERGY (E)** = 9V, **RESISTANCE (R)** = 9kΩ and **CAPACITOR (C)** = 1nF

(3 marks)

(c) Determine **CAPACITOR EXTERNAL** (C_{ext}) for monostable (One-Shot) if given **ENERGY (E)** = 12V, **TIME WIDTH** (t_w) = 0.1s and **RESISTANCE (R)** = 39kΩ

(3 marks)

(d) For the astable multivibrator, if R_1=1 MΩ, R_2= 470 kΩ and C_1=0.001 μF, determine the frequency output, **TIME HIGH** (t_{HI}), **TIME LOW** (t_{LO}) and duty cycle.

(8 marks)

Q7 (a) Convert each of the BCD code 0000, 0010, 0100, 0110, 0111 to Gray Code.

(3 marks)

(b) Design a J-K synchronous 3-bit up/down counter with a Gray code sequence from part **Q7** (a). The counter should count up when an UP/$\overline{\text{DOWN}}$ control input is 1 and count down when the control input is 0.

(17marks)

Q8 (a) Determine the output Q_0,Q_1,Q_2 and Q_3 of 74HC194 IC a 4-bit bidirectional universal shift register if given the data input waveforms as shown in Figure **Q8** (a).

(14 marks)

(b) If a 10-bit ring counter in Figure **Q8** (b) has the initial state 0101001111, determine the waveform for each of the Q outputs.

(6marks)

Q9 (a) Determine the Boolean expression of X for the circuit in Figure **Q9** (a).

(4 marks)

(b) Convert the Boolean expression from part Q9 (a) into a standard SOP expression. (show all your steps)

(6 marks)

(c) Use Karnaugh map to determine the minimum SOP expression for X. (show all your steps)

(10 marks)

Q10 (a) By referring to the logic schematic J-K flip-flop in Figure **Q10** (a), determine the output $\overline{Q}$ if the input waveforms CLK, J, K, Clear and Preset. Q is initially 1.

(10 marks)

(b) Determine the waveforms at Q, $\overline{Q}$(Q'), CP and $\overline{CP}$(CP') in Figure **Q10** (b) for a non-overlapping clock.

(10 marks)

FINAL EXAMINATION

SEMESTER / SESSION : SEMESTER II / 2009/2010
COURSE NAME : LOGIC SYSTEM
PROGRAMME : 2 DET / DEE / DEX
COURSE CODE : DEE2223

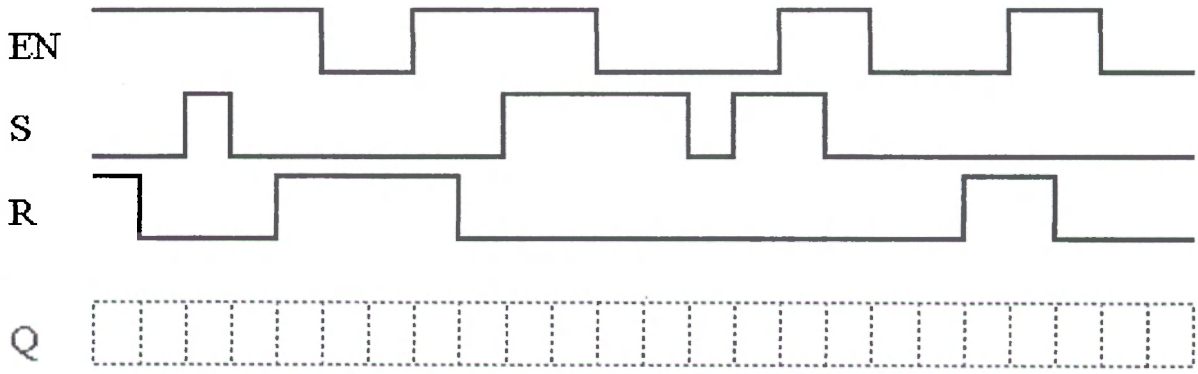
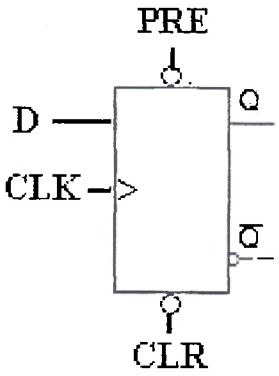


Figure Q1(d)

FINAL EXAMINATION

SEMESTER / SESSION : SEMESTER II / 2009/2010
COURSE NAME : LOGIC SYSTEM
PROGRAMME : 2 DET / DEE / DEX
COURSE CODE : DEE2223



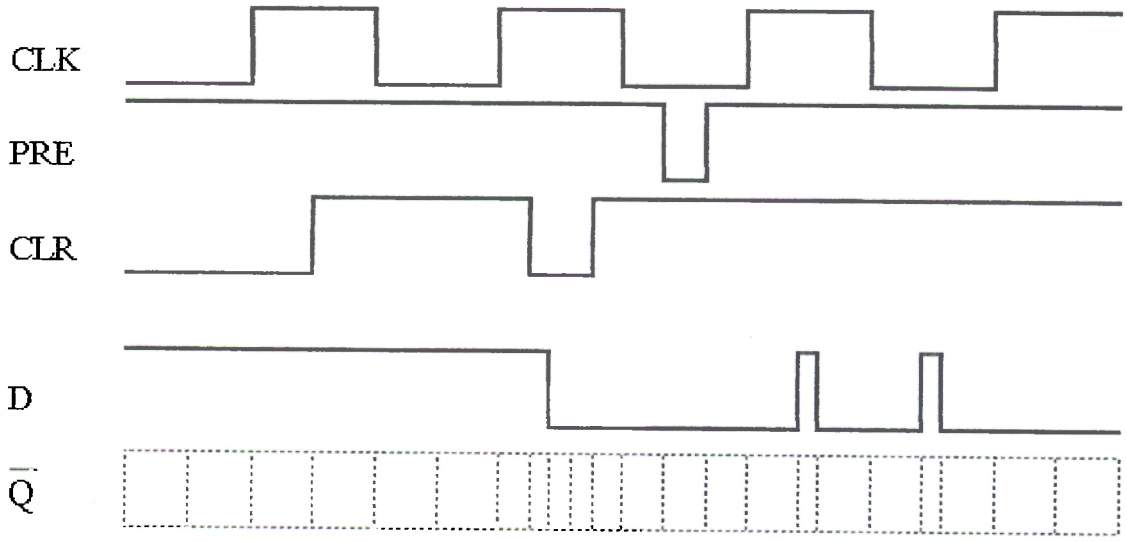


Figure **Q2**(d)

FINAL EXAMINATION

SEMESTER / SESSION : SEMESTER II / 2009/2010
COURSE NAME : LOGIC SYSTEM
PROGRAMME : 2 DET / DEE / DEX
COURSE CODE : DEE2223

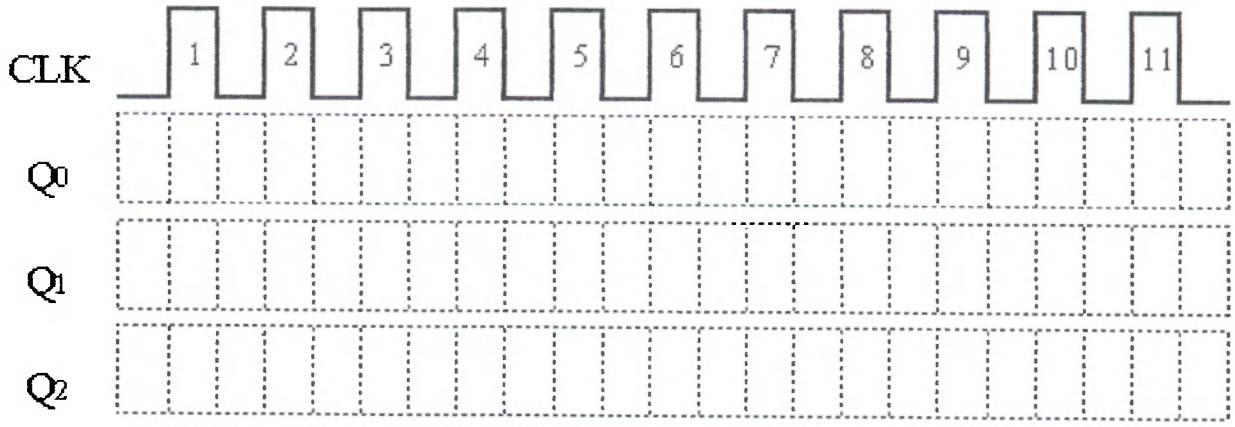


Figure **Q3** (a)

FINAL EXAMINATION

SEMESTER / SESSION : SEMESTER II / 2009/2010
COURSE NAME : LOGIC SYSTEM
PROGRAMME : 2 DET / DEE / DEX
COURSE CODE : DEE2223

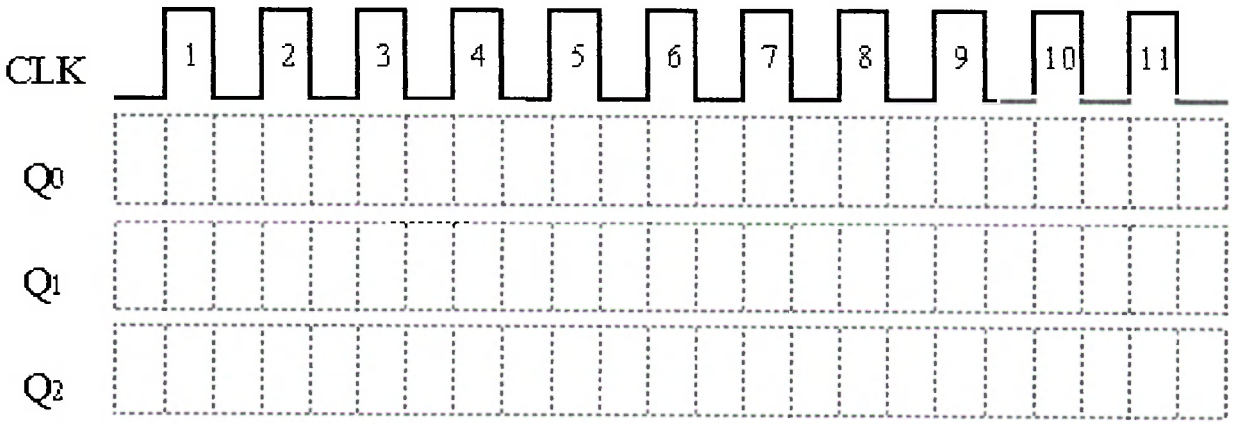


Figure **Q3** (c)

FINAL EXAMINATION

SEMESTER / SESSION : SEMESTER II / 2009/2010
COURSE NAME : LOGIC SYSTEM
PROGRAMME : 2 DET / DEE / DEX
COURSE CODE : DEE2223

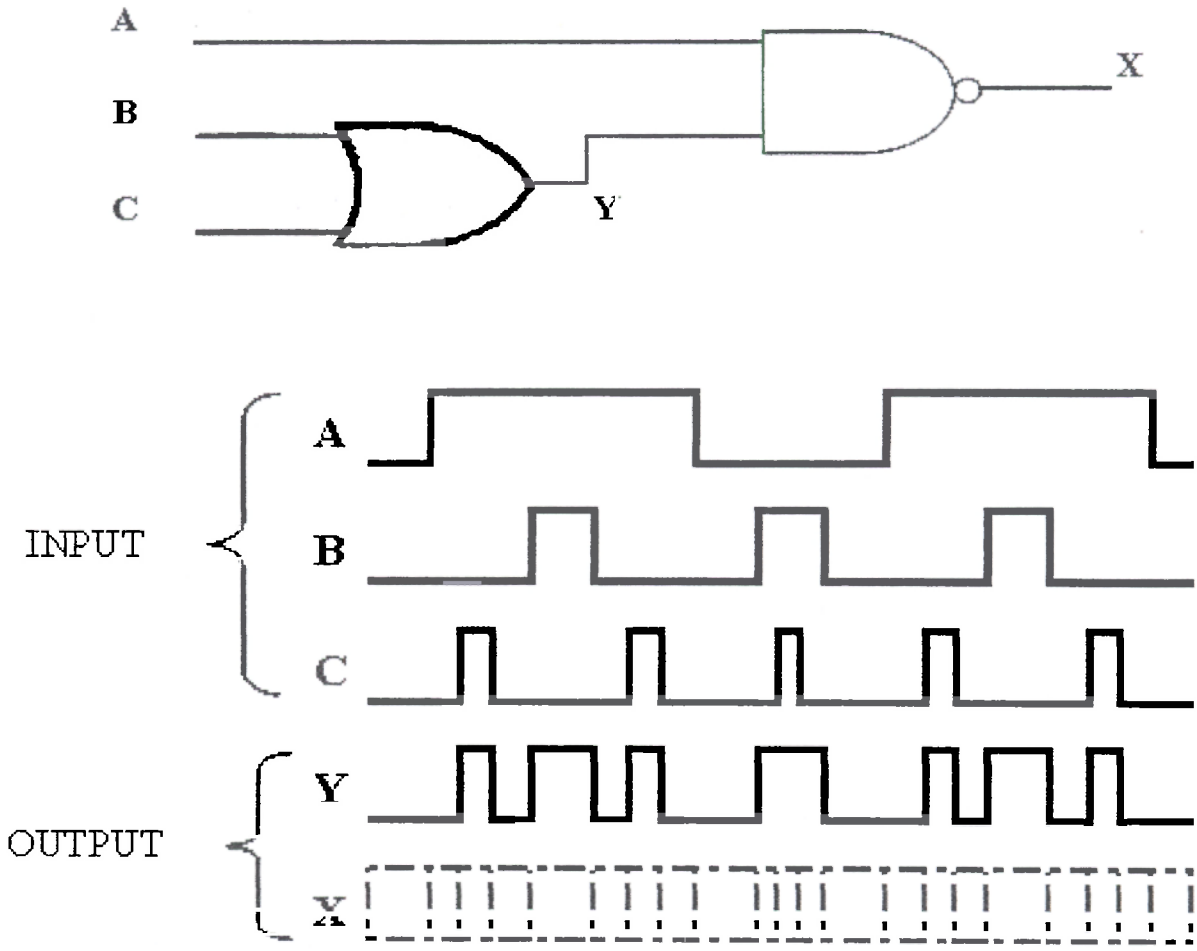
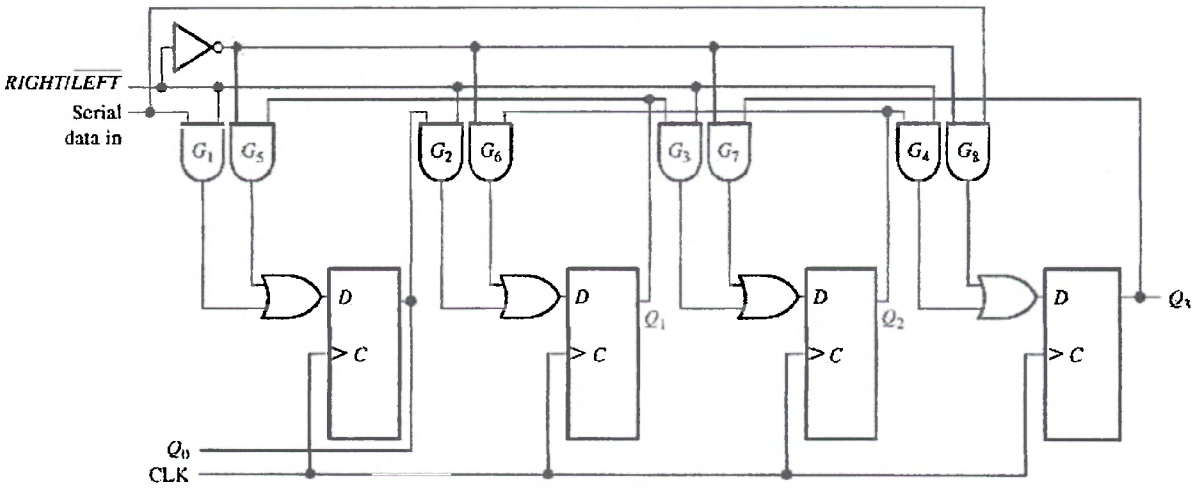


Figure **Q4** (c)

FINAL EXAMINATION

SEMESTER / SESSION : SEMESTER II / 2009/2010
COURSE NAME : LOGIC SYSTEM
PROGRAMME : 2 DET / DEE / DEX
COURSE CODE : DEE2223



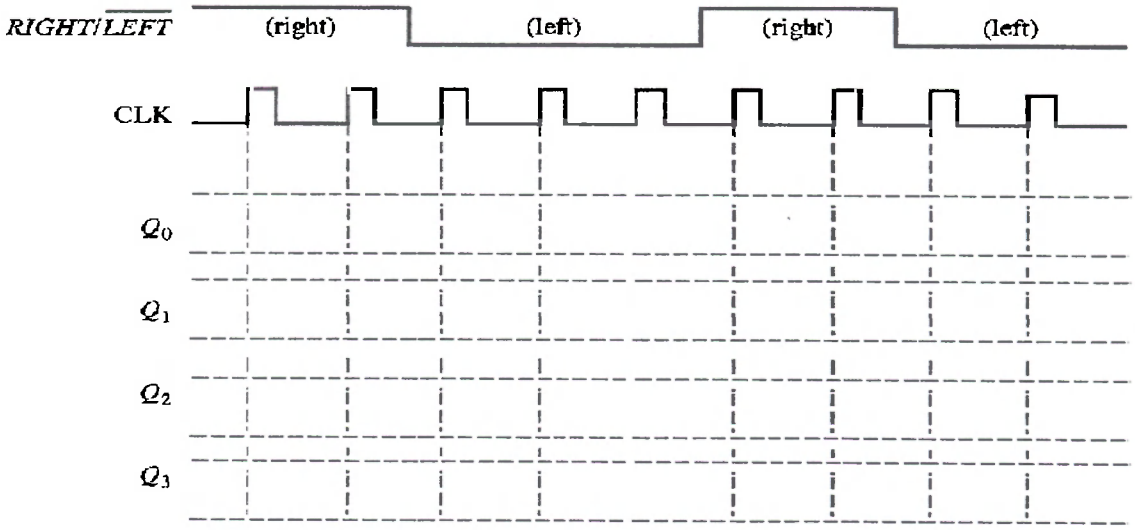


Figure **Q5** (b)

FINAL EXAMINATION

SEMESTER / SESSION : SEMESTER II / 2009/2010
COURSE NAME : LOGIC SYSTEM
PROGRAMME : 2 DET / DEE / DEX
COURSE CODE : DEE2223

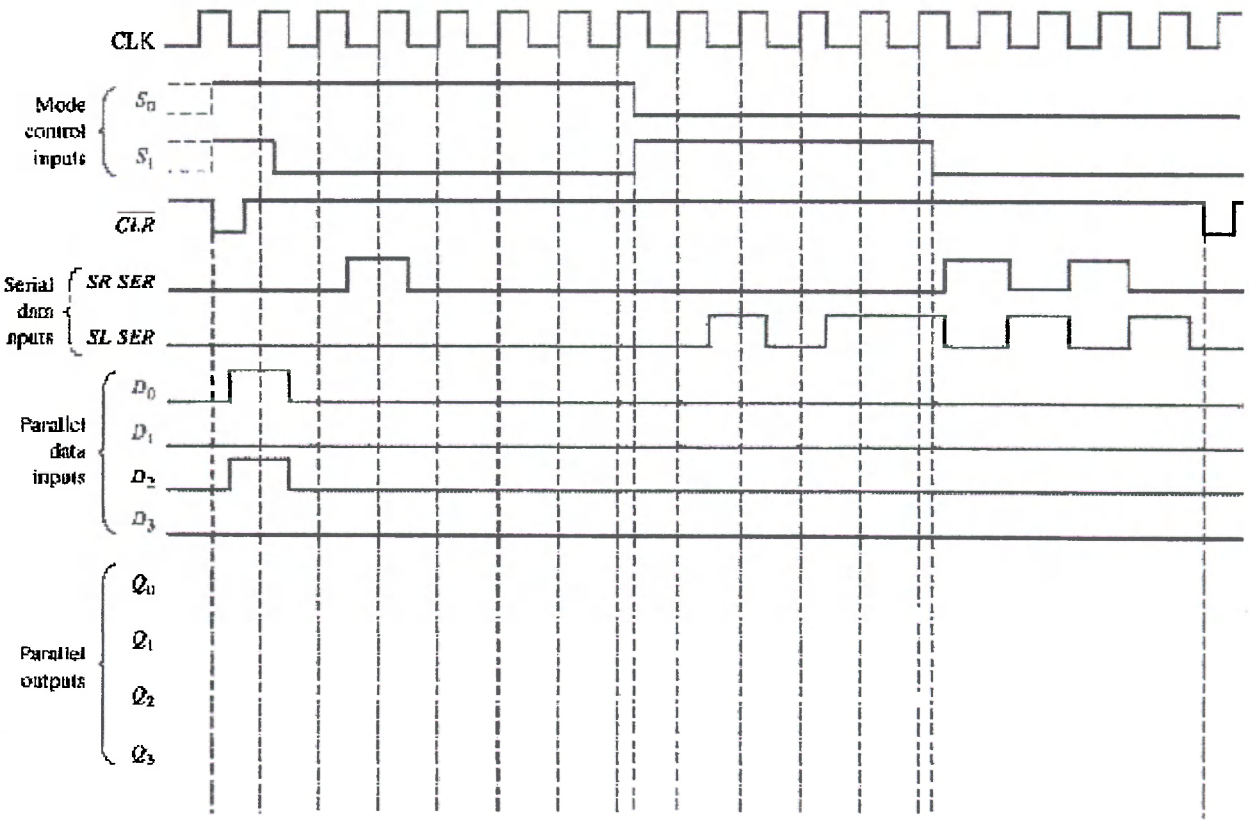


Figure **Q8**(a)

FINAL EXAMINATION

SEMESTER / SESSION : SEMESTER II / 2009/2010
COURSE NAME : LOGIC SYSTEM
PROGRAMME : 2 DET / DEE / DEX
COURSE CODE : DEE2223

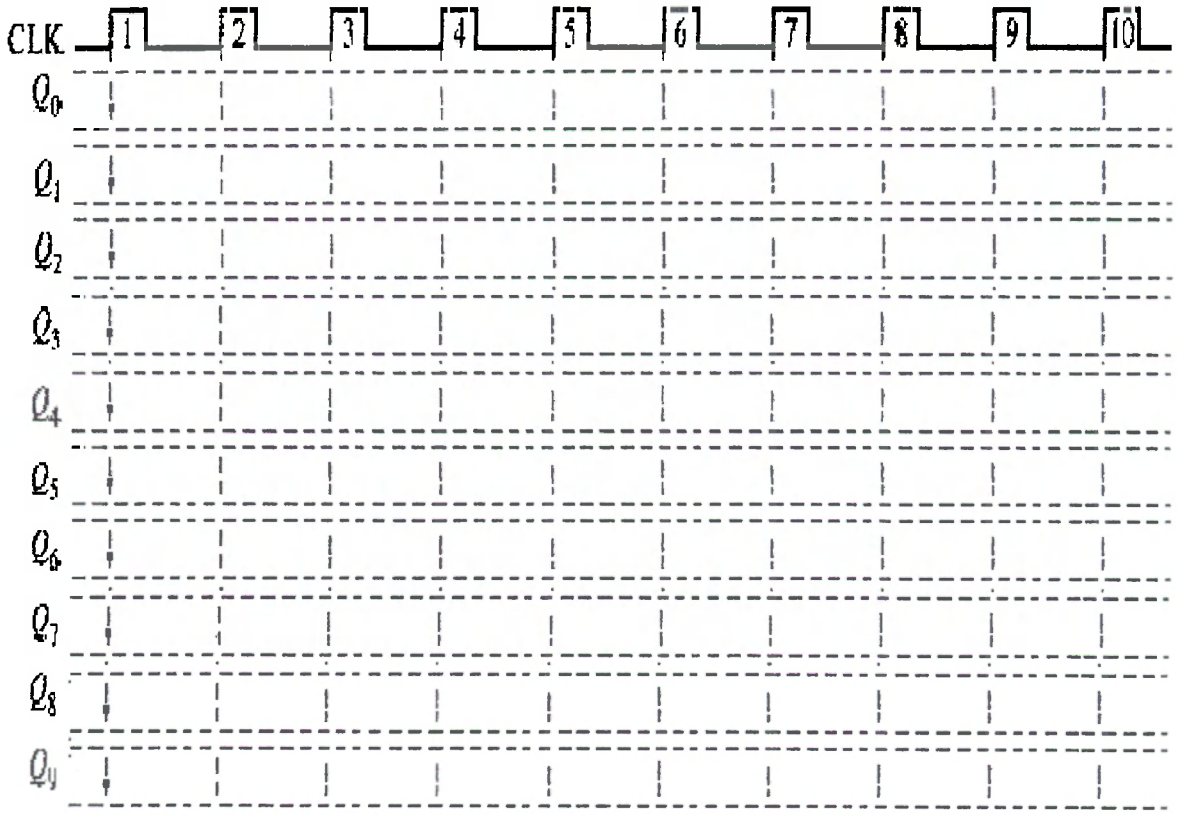


Figure **Q8**(b)

FINAL EXAMINATION

SEMESTER / SESSION : SEMESTER II / 2009/2010
COURSE NAME : LOGIC SYSTEM
PROGRAMME : 2 DET / DEE / DEX
COURSE CODE : DEE2223

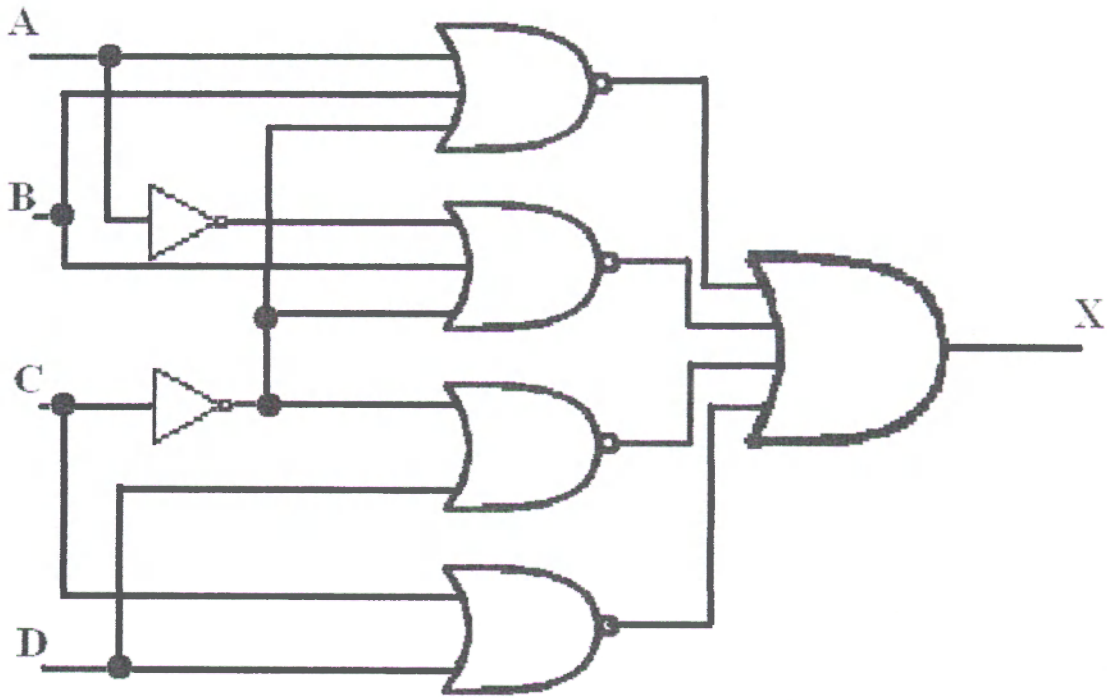
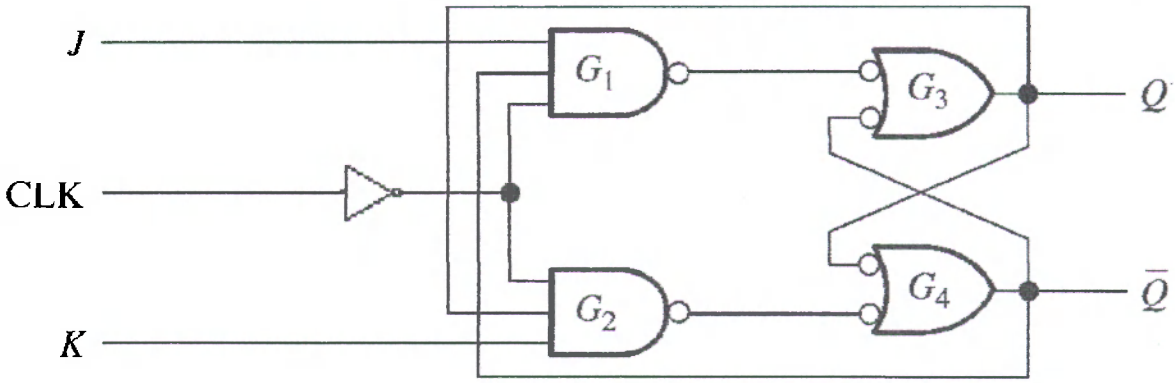


Figure **Q9** (a)

FINAL EXAMINATION

SEMESTER / SESSION : SEMESTER II / 2009/2010
COURSE NAME : LOGIC SYSTEM
PROGRAMME : 2 DET / DEE / DEX
COURSE CODE : DEE2223



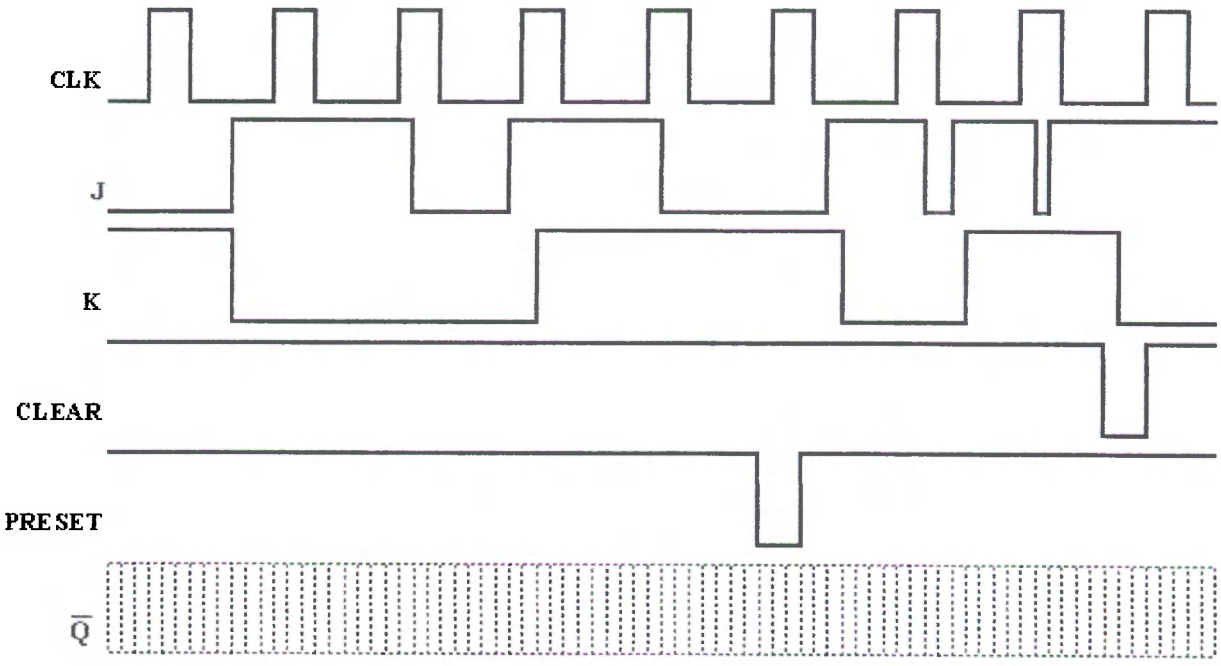
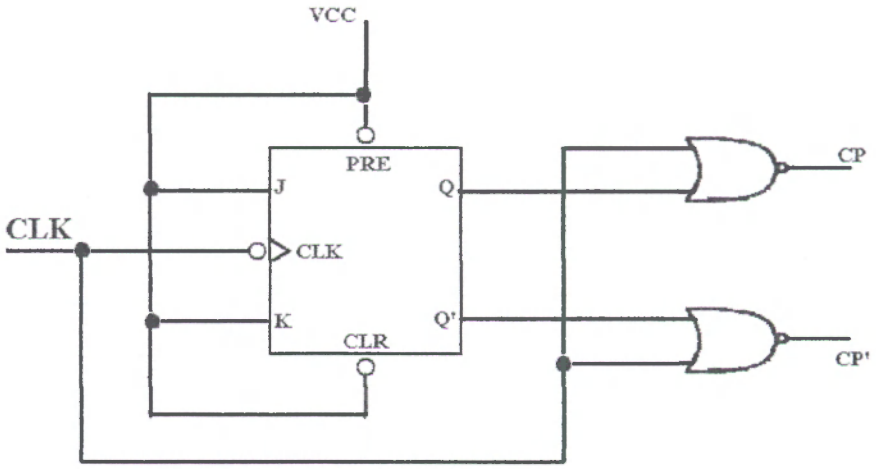


Figure Q10(a)

FINAL EXAMINATION

SEMESTER / SESSION : SEMESTER II / 2009/2010
COURSE NAME : LOGIC SYSTEM
PROGRAMME : 2 DET / DEE / DEX
COURSE CODE : DEE2223



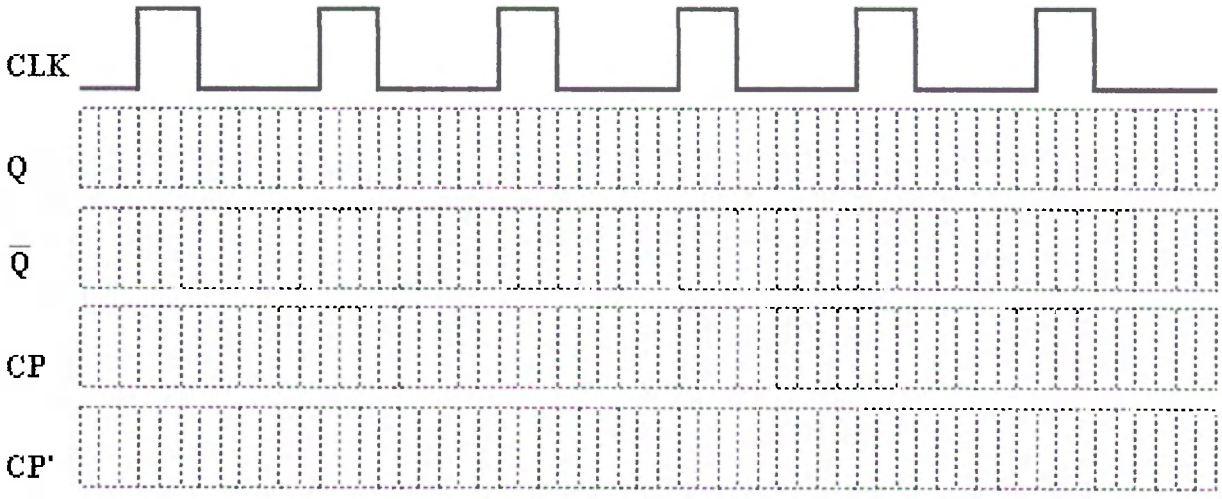


Figure **Q10** (b)