UNIVERSITI TUN HUSSEIN ONN MALAYSIA

FINAL EXAMINATION
SEMESTER II
SESSION 2010/2011

COURSE NAME	:	ELECTRONICS CIRCUITS
COURSE CODE	:	BEF 12603
PROGRAMME	:	BEF
EXAMINATION DATE	:	APRIL/MAY 2011
DURATION	:	2 HOURS 30 MINUTES
INSTRUCTION	:	ANSWER **FOUR (4)** QUESTIONS ONLY

THIS PAPER CONSISTS OF ELEVEN(11) PAGES

Q1 a) Describe the operation of NPN bipolar-transistor using appropriate diagrams.
(6 marks)

b) Which of the transistor currents is the largest? Which is always the smallest? Which two currents are relatively close in magnitude?
(3 marks)

c) Referring to the circuit shown in Figure Q1(c) determine I_B for $\beta = 95$. Hence, find the quiescent points, I_{CQ} and V_{CEQ}.
(8 marks)

d) Using the same circuit of Figure Q1(c), re-calculate I_{CQ} and V_{CEQ} for new value of $\beta = 140$. Hence discuss in brief the new results obtained.
(8 marks)

Q2 a) Sketch the circuit configuration of :

(i) BJT DC emitter bias
(ii) BJT common-base bias configuration.
(4 marks)

b) Figure Q2(b) shows the operating region of BJT. Discuss the characteristics of each region.
(8 marks)

c) Referring to Figure Q2(c), use exact analysis technique to verify the expression of I_B and V_{CE} as stated below.

$$I_B = \frac{V_{TH} - V_{BE}}{R_{TH} + (\beta + 1)R_E}$$

$$V_{CE} = V_{CC} - I_C(R_C + R_E)$$ *Note: use Thevenin theorem.*
(7 marks)

d) Figure Q2(d)(i) shows the BJT characteristic curve with load-line that gives an operating point (Q-point) of $I_{CQ} = 3.735\text{mA}$ and $V_{CEQ} = 4.63\text{V}$. Say it is related to the DC bias configuration as shown in Figure Q2(d)(ii), calculate V_{EE}, R_B and R_C if $V_{EE} = 1.5V_{CEQ}$.
(6 marks)

Q3 a) Sketch characteristic curves of BJT and MOSFET. Label all important parameters completely. Discuss the characteristic differences between the two.

(6 marks)

b) Discuss the advantages and disadvantage of MOSFET

(6 marks)

c) For a certain D-MOSFET, I_{DSS} = 12mA and $V_{GS(off)}$ = -9V

i) Is this an n-channel or p-channel type?
ii) Calculate I_D at V_{GS} = - 4V
iii) Calculate I_D at V_{GS} = +4V

(5 marks)

d) For the n-channel depletion-type MOSFET of Figure Q3(d), determine:

i) I_{DQ} and V_{GSQ}
ii) V_{DS}

(8 marks)

Q4 a) Sketch transconductance curves of JFET and D-MOSFET. Label all important parameters completely. Discuss the characteristic differences between the two.

(6 marks)

b) Referring to the configuration of network in Figure Q4(b), derive the following expressions :

i) Gate voltage, V_G
ii) Gate-source voltage, V_{GS}
iii) Drain current, I_D at V_{GS} = 0

(8 marks)

c) Calculate the value of source resistance, R_S required to self-bias a JFET with datasheet values of I_{DSS} = 25mA and V_P = 15V. V_{GS} is to be 5V.

(4 marks)

d) Determine the quiescent point (Q-point) for the network of Figure Q4(d). Given, for this particular JFET, the parameter values are such that $V_D \approx 7V$.

(7 marks)

Q5 a) Draw the equivalent of a transistor network as shown in Figure Q5(a) for small-signal ac analysis.

(4 marks)

b) Figure Q5(b) shows the BJT amplifier, represented in two port system. Calculate the followings :

i) Input voltage, V_i,
ii) Input current, I_i,
iii) Input impedance, Z_i,
iv) Voltage gain, A_v

(4 marks)

c) For a common-base configuration shown in Figure Q5(c), with $I_E = 5.3\text{mA}$ and $\alpha = 0.92$ and an ac signal of 2.7mV applied between base and emitter terminals :

i) Calculate the input impedance
ii) Find the voltage gain if a load of 770Ω is connected to the output terminals
iii) Find the output impedance and the current gain.

(8 marks)

d) For the circuit configuration of Figure Q5(d) calculate the followings:

i) Calculate equivalent resistance r_e,
ii) Determine input impedance Z_i (with $r_o = \infty\Omega$)
iii) Find output impedance Z_o (with $r_o = \infty\Omega$)
iv) Calculate voltage gain A_V (with $r_o = \infty\Omega$)
v) Find current gain A_i (with $r_o = \infty\Omega$)

(9 marks)

Q6 a) Discuss in your own words about operational amplifier. State also typical applications of op-amp.

(8 marks)

b) Define Common-Mode Rejection Mode (CMRR).

(3 marks)

c) Identify each of the op-amp configurations in Figure Q6(c).

(3 marks)

d) A certain op-amp has an open-loop differential voltage gain of 150,000 and a common-mode gain of 0.25. Determine the common-mode rejection ratio (CMRR) and express it in decibels.

(3 marks)

e) Referring to the amplifier in Figure Q6(e) :

i) Determine the input and output impedances given in the op-amp datasheet shows $Z_{in} = 1.5M\Omega$, $Z_{out} = 67\Omega$ and $A_{ol} = 222{,}000$

ii) Find the closed-loop voltage gain

(5 marks)

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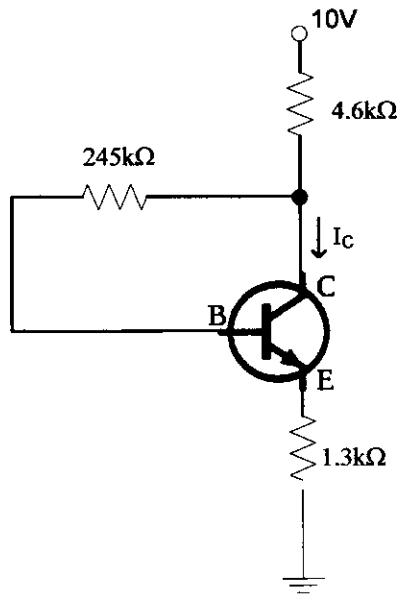

Figure Q1(c)

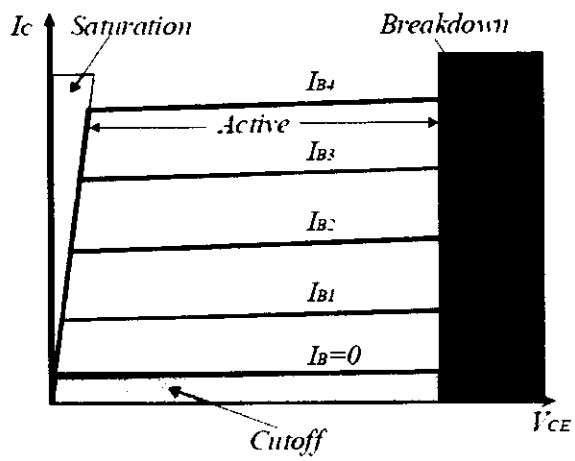

Figure Q2(b)

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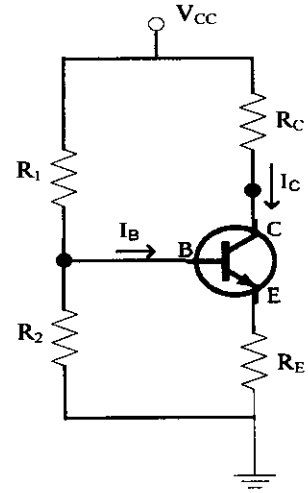

Figure 2(c)

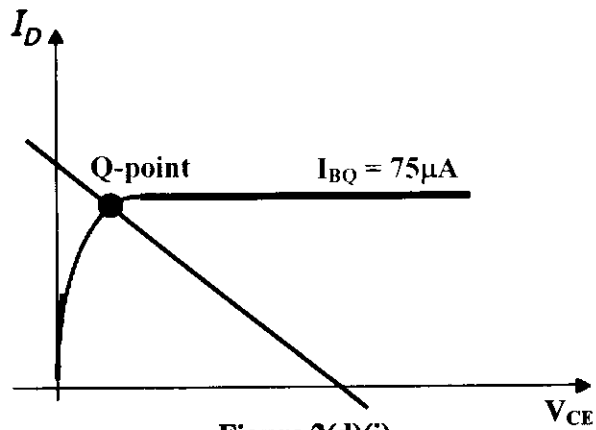

Figure 2(d)(i)

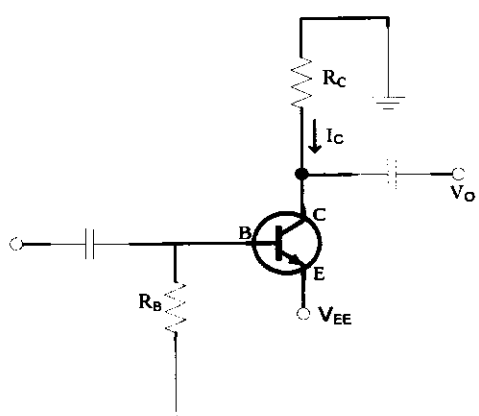

Figure 2(d)(ii)

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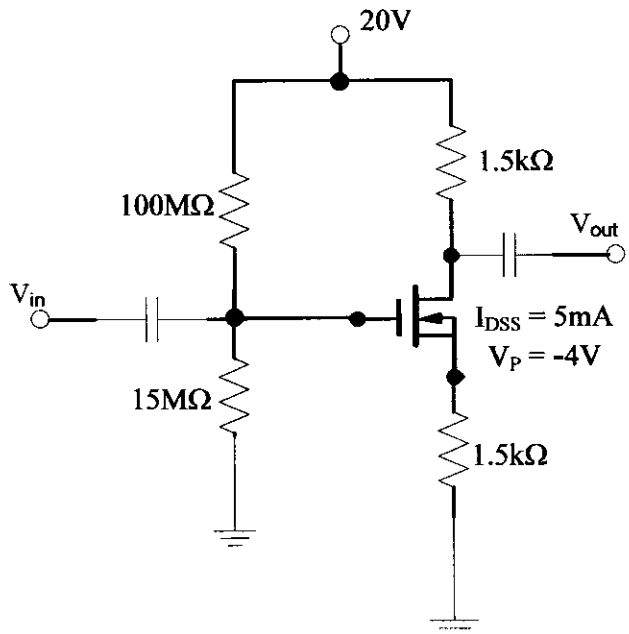

Figure Q3(d)

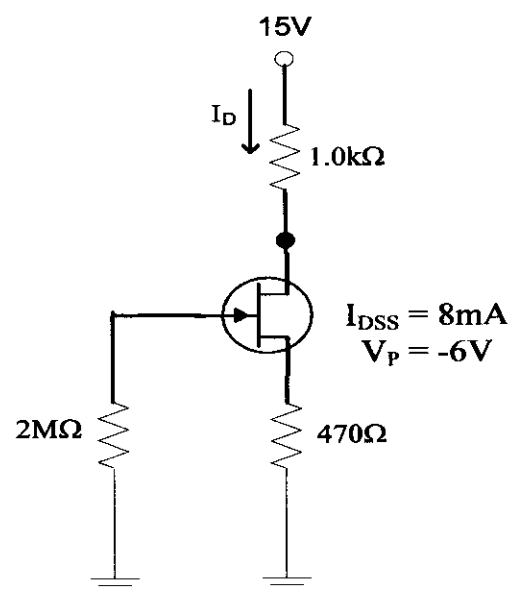

Figure Q4(c)

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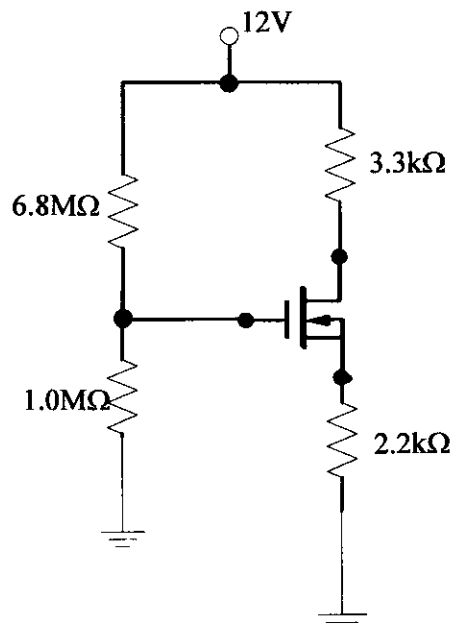

Figure Q4(d).

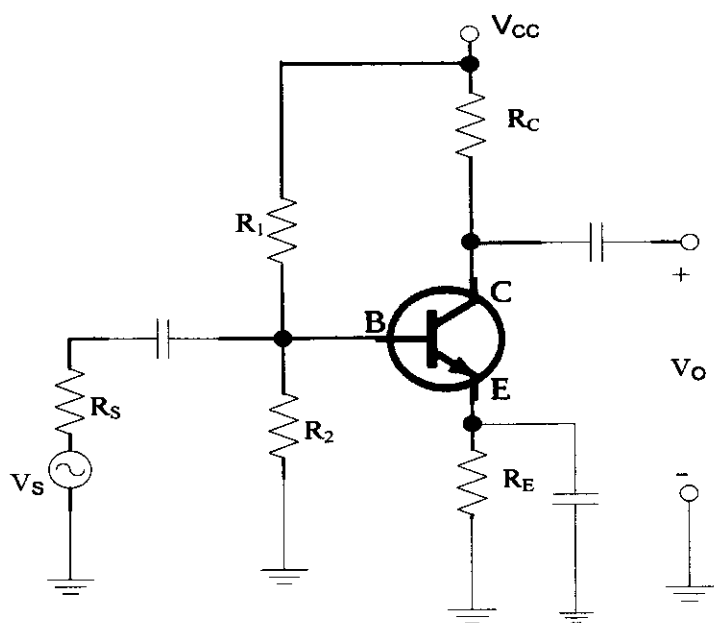

Figure Q5(a)

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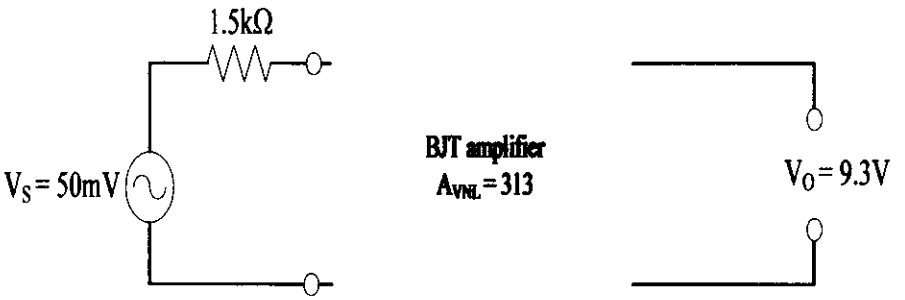

Figure Q5(b)

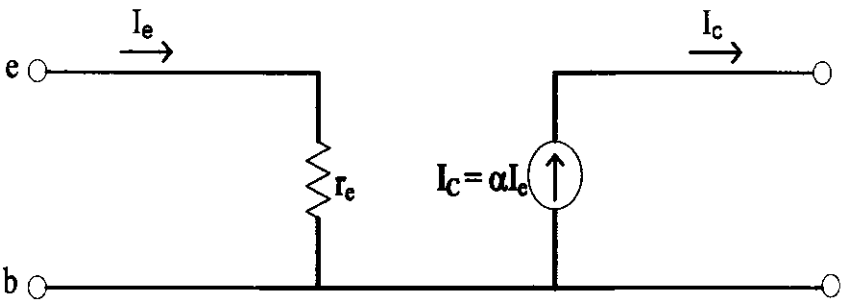

Figure Q5(c)

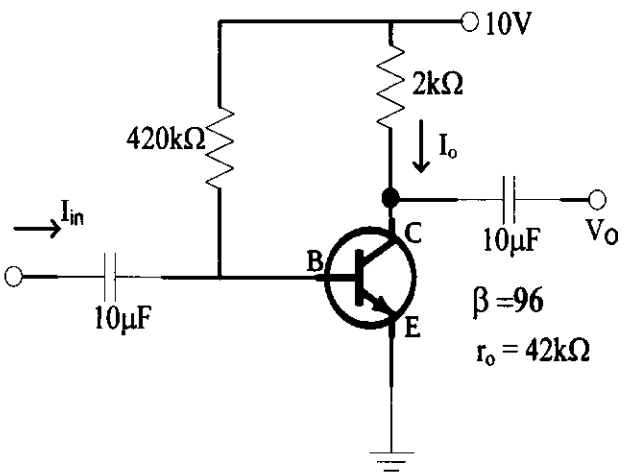

Figure Q5(d)

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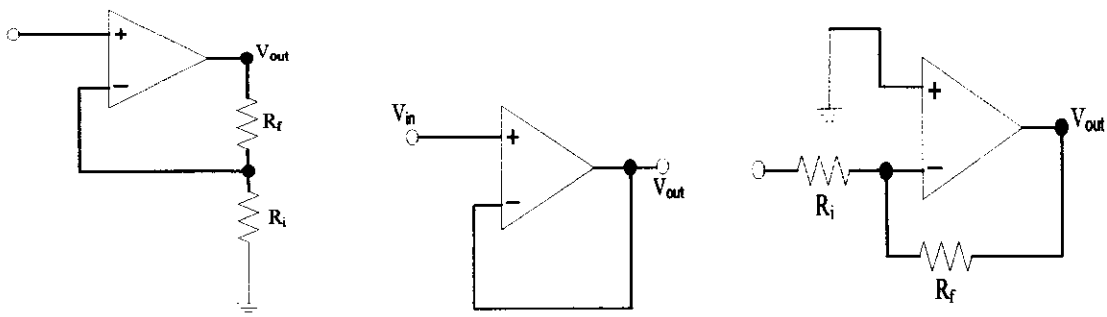

Figure Q6(c)

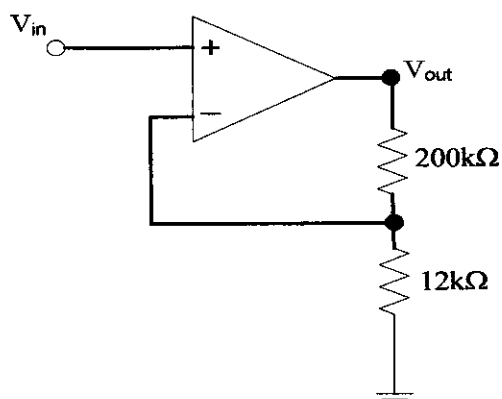

Figure Q6(e)