UNIVERSITI TUN HUSSEIN ONN MALAYSIA

FINAL EXAMINATION
SEMESTER II
SESSION 2011/2012

COURSE NAME	:	ANALOG ELECTRONICS / ELECTRONIC PRINCIPLES
COURSE CODE	:	BEL 10203 / BEE 2113
PROGRAMME	:	BED / BEB / BEH / BEC / BEU / BEE
EXAMINATION DATE	:	JUNE 2012
DURATION	:	3 HOURS
INSTRUCTION	:	ANSWER **FIVE (5)** QUESTIONS ONLY

THIS PAPER CONSISTS OF **TEN** (10) PAGES

Q1. (a) Explain what is meant by intrinsic semiconductor and extrinsic semiconductor material.

(4 marks)

(b) Describe briefly the function of the following diode circuits:

(i) Rectifier

(2 marks)

(ii) Clamper

(2 marks)

(c) Draw and label the output voltage, V_o for the circuit in **Figure Q1(c)(i)** for each input voltage shown in **Figure Q1(c)(ii)** and **Figure Q1(c)(iii).** Assume that silicon diodes are used. Name the circuit used and explain its operation.

(12 marks)

Q2. (a) A bridge rectifier with a 10 kΩ load is driven by a transformer with 10:1 turn ratio. The primary transformer is connected to a 240 V, 50 Hz mains supply.

(i) Draw the schematic diagram of the circuit

(3 marks)

(ii) Draw and label the input and output voltage waveforms of the rectifier.

(4 marks)

(iii) Calculate the dc load voltage, V_{dc} and current values, I_{dc}.

(3 marks)

(b) For the voltage regulator circuit in **Figure Q2(b)**, let V_{in} = 6.3 V, R_S = 12 Ω, and V_z = 4.8 V. The zener diode current, I_z is limited to the range between 5 mA and 100 mA.

(i) Determine the range of possible load currents, I_L and load resistances, R_L.

(7 marks)

(ii) Determine the power rating required for the zener diode, P_z and the power dissipated by load resistor, P_L.

(3 marks)

Q3. (a) Referring to **Figure Q3(a),** given $\beta = 80$ and $r_o = 40$ kΩ.

(i) Draw the AC equivalent circuit using r_e model.

(3 marks)

(ii) Determine the AC dynamic resistance, r_e.

(6 marks)

(iii) Determine the input impedance, Z_i and output impedance, Z_o for the circuit.

(4 marks)

(iv) Calculate the voltage gain, A_v.

(2 marks)

(b) Briefly describe the frequency response of an amplifier. Use an appropriate diagram to support your explanations.

(5 marks)

Q4. Referring to the circuit in **Figure Q4**, given:

$C_{be} = 35$ pF, $C_{bc} = 4$ pF, $C_{ce} = 1$ pF, $C_{Wi} = 5$ pF, $C_{Wo} = 8$ pF
$C_S = 10$ µF, $C_E = 20$ µF, $C_C = 1$ µF

$R_1 = 39$ kΩ, $R_2 = 10$ kΩ, $R_C = 3.9$ kΩ, $R_E = 2.2$ kΩ, $R_S = 1$ kΩ, $R_L = 2.2$ kΩ
$\beta = 100$, $r_o = \infty$ Ω, $V_{cc} = 20$ V

(a) Determine the AC dynamic resistance, r_e.

(5 marks)

(b) Find the lower cutoff frequencies f_{LS}, f_{LC} dan f_{LE} due to coupling capacitors and bypass capacitor.

(6 marks)

(c) Find the upper cutoff frequencies, f_{Hi}, f_{Ho} dan f_β.

(6 marks)

(d) Sketch the frequency response which includes both the low and high frequency regions using the results obtained in part Q4(b) and part Q4(c).

(3 marks)

Q5. **Figure Q5** shows a circuit diagram of JFET amplifier with following parameters: I_{DSS} = 8 mA, V_p = -8 V and $r_d = \infty\ \Omega$. Determine:

(a) Drain current, I_{DQ} and gate-to-source voltage, V_{GSQ} at quiescent point.

(5 marks)

(b) Input impedance, Z_i and output impedance, Z_o

(2 marks)

(c) Transconductance, g_m and midband gain, A_{vmid}

(3 marks)

(d) AC small signal model for the amplifier circuit

(2 marks)

(e) Low cutoff frequency, f_L.

(4 marks)

(f) High cutoff frequency, f_H.

(4 marks)

Q6. (a) Draw the transfer characteristics curve of a JFET, D-MOSFET and an E-MOSFET and describe the differences among them.

(6 marks)

(b) **Figure Q6(b)** shows the graphically method for determining the Q-point for an n-channel enhancement type MOSFET.

(i) Design a circuit by using voltage-divider biasing arrangement that will give the result as shown in **Figure Q6(b)**. Given V_{DD} = 40V, R_2 = 18MΩ and V_D = 20V.

(9 marks)

(ii) Find V_{DS} and $V_{GS\,(TH)}$.

(3 marks)

(iii) Determine the resulting value of k for the MOSFET.

(2 marks)

Q7 (a) For the Darlington pair circuit in **Figure Q7(a)**, given $\beta_D = 6000$ and $V_{BE} = 1.6$ V.

(i) Calculate the dc bias voltage, V_{E2} and emitter current, I_{E2}.

(4 marks)

(ii) Determine the output voltage, V_o.

(6 marks)

(b) **Figure Q7(b)** shows a differential amplifier. Assuming that all the transistors in the circuit are very well matched and $V_{BE} = 0.7$ V, $\beta = 75$. Determine:

(i) The current, I.

(3 marks)

(ii) The common mode gain, A_{cm} and differential gain, A_d.

(4 marks)

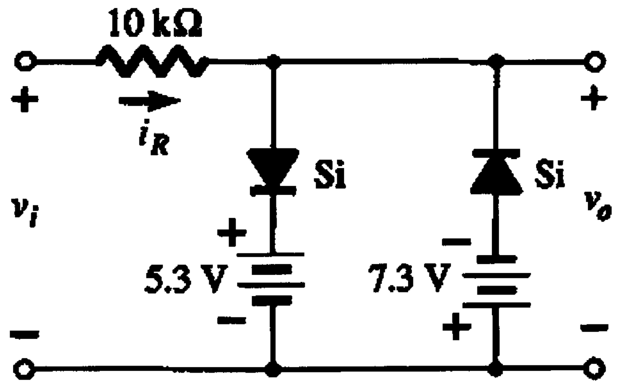
(iii) The common-mode rejection ratio (CMRR) in dB.

(3 marks)

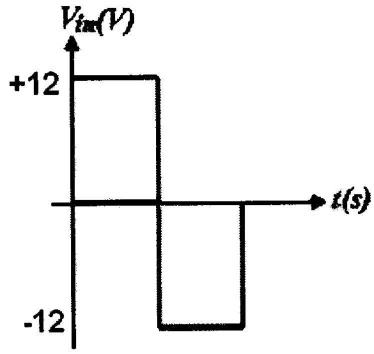
FINAL EXAMINATION

SEMESTER/SESSION: SEM II / 2011/2012
COURSE: ANALOG ELECTRONICS/
ELECTRONIC PRINCIPLES

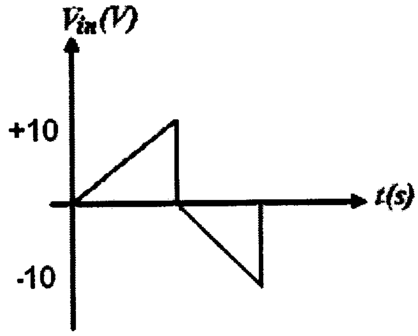
PROGRAMME: BEB/ BEC/ BEH/ BED/ BEU/ BEE
COURSE CODE: BEL10203/BEE2113



(i)



(ii)



(iii)

FIGURE Q1(c)

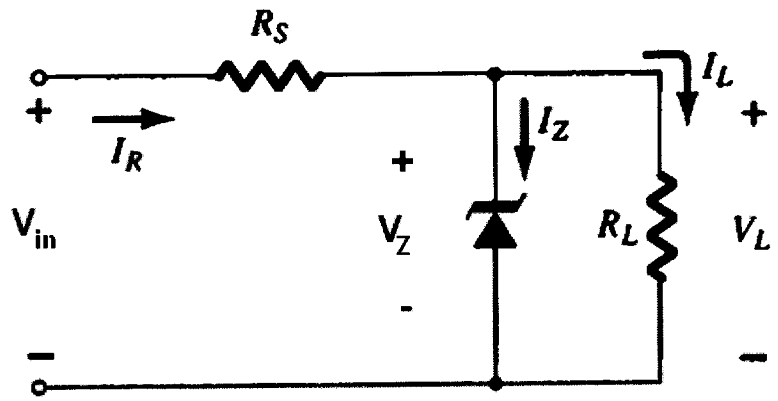


FIGURE Q2(b)

FINAL EXAMINATION

SEMESTER/SESSION: SEM II / 2010/2011
COURSE: ANALOG ELECTRONICS/ ELECTRONIC PRINCIPLES

PROGRAMME: BEB/ BEC/ BEH/ BED/ BEU/ BEE
COURSE CODE: BEL10203/BEE2113

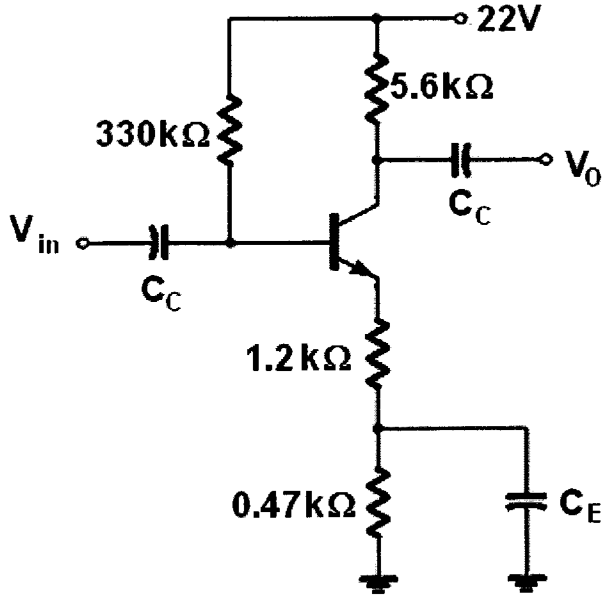


FIGURE Q3(a)

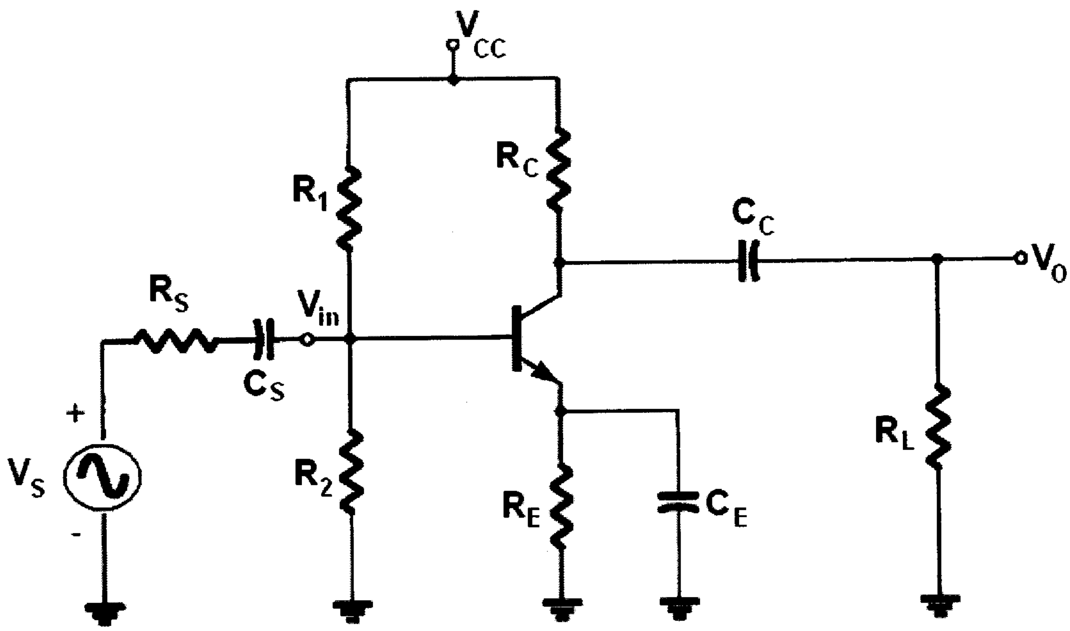


FIGURE Q4

FINAL EXAMINATION

SEMESTER/SESSION: SEM II / 2010/2011
COURSE: ANALOG ELECTRONICS/
ELECTRONIC PRINCIPLES

PROGRAMME: BEB/ BEC/ BEH/ BED/ BEU/ BEE
COURSE CODE: BEL10203/BEE2113

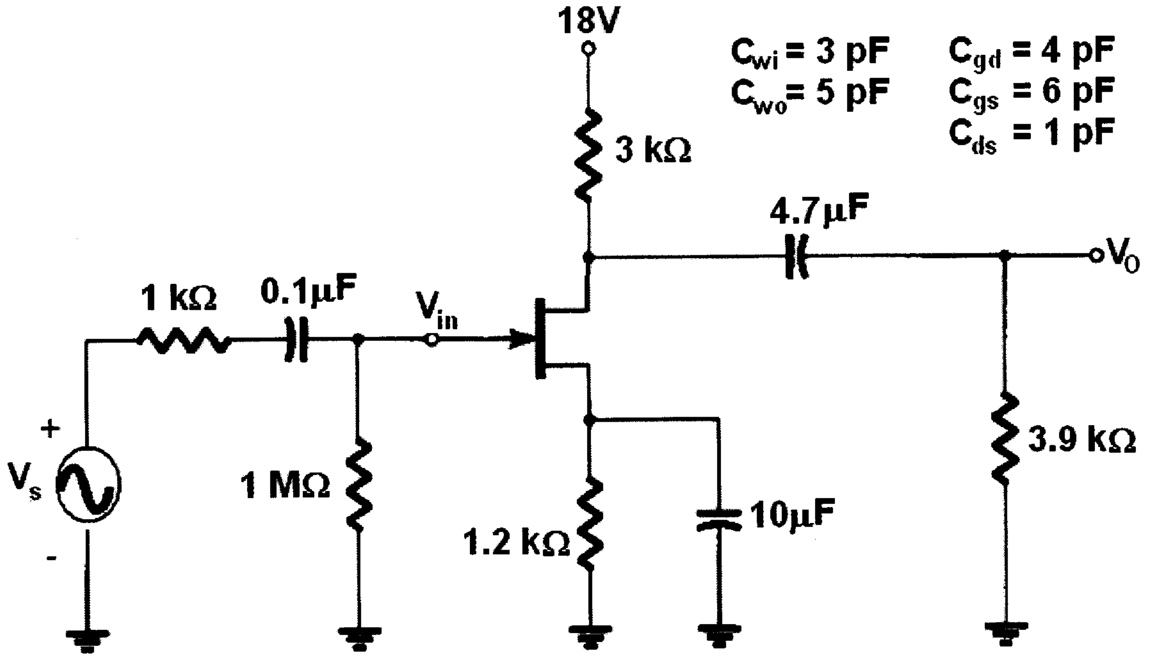


FIGURE Q5

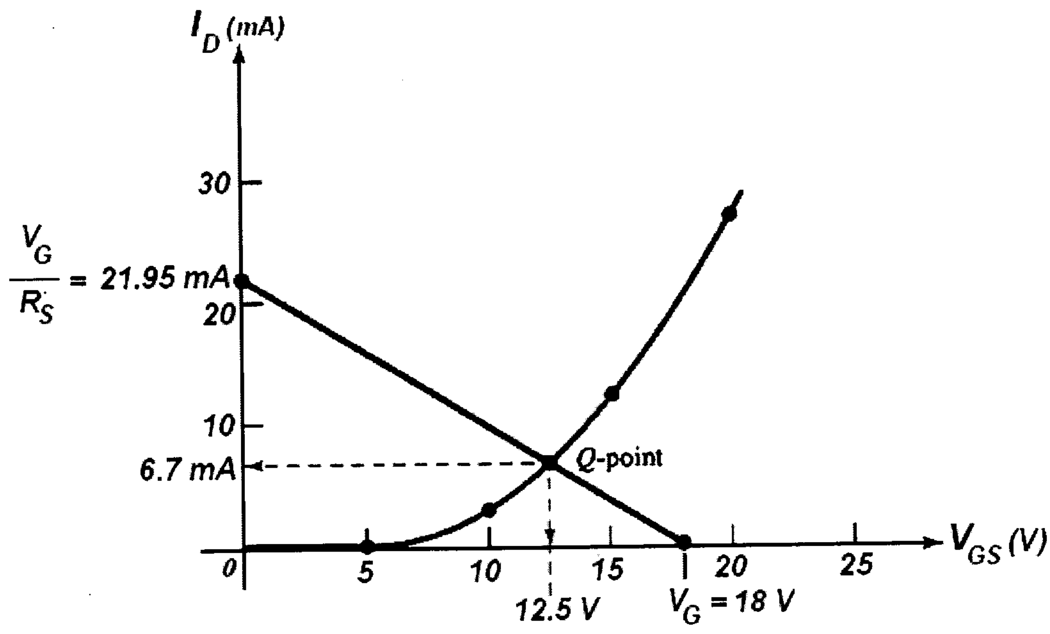


FIGURE Q6(b)

FINAL EXAMINATION

SEMESTER/SESSION: SEM II / 2010/2011
COURSE: ANALOG ELECTRONICS/
ELECTRONIC PRINCIPLES

PROGRAMME: BEB/ BEC/ BEH/ BED/ BEU/ BEE
COURSE CODE: BEL10203/BEE2113

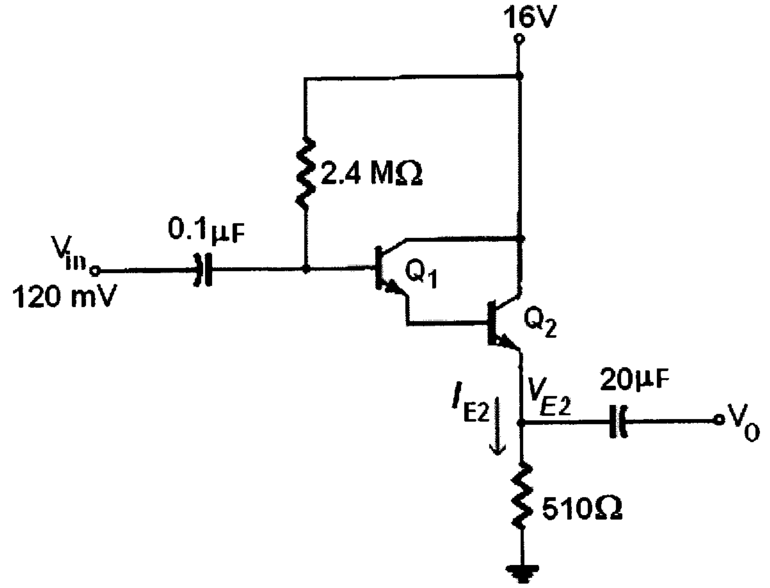


FIGURE Q7(a)

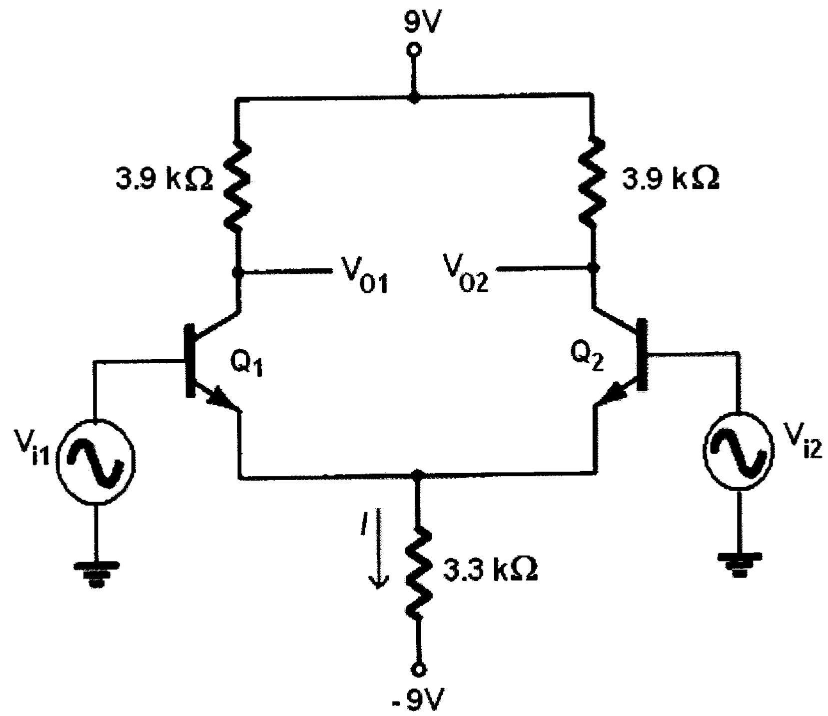


FIGURE Q7(b)

FINAL EXAMINATION

SEMESTER/SESSION: SEM II / 2010/2011
COURSE: ANALOG ELECTRONICS/
ELECTRONIC PRINCIPLES

PROGRAMME: BEB/ BEC/ BEH/ BED/ BEU/ BEE
COURSE CODE: BEL10203/BEE2113

LIST OF FORMULAE:

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2$$

$$I_D = k\left(V_{GS} - V_{GS(TH)}\right)^2$$