UNIVERSITI TUN HUSSEIN ONN MALAYSIA

FINAL EXAMINATION
SEMESTER II
SESSION 2012/2013

COURSE NAME	:	DIGITAL SYSTEM DESIGN
COURSE CODE	:	BEE 3133/BEX31503
PROGRAMME	:	3 BEE
EXAMINATION DATE	:	JUNE 2013
DURATION	:	3 HOURS
INSTRUCTION	:	ANSWER **ALL** QUESTIONS

THIS QUESTION PAPER CONSISTS OF **SIX (6)** PAGES

Q1 (a) In 1965, Gordon Moore predict that the transistor would continue to shrink

(i) Identify THREE (3) advantages on electronic device capabilities based on this prediction.

(3 marks)

(ii) Moore's Law has proved remarkably accurate for more than half a century, but it is expected that the growth will slow by the end of 2013. Predict TWO (2) restrictions that should be considered in Moore's Law.

(3 marks)

(b) Based on VHDL code in Figure Q1 (b), construct its schematic circuit.

(7 marks)

(c) By using 'Case Statement', compose the VHDL code for 5-to-1 multiplexer circuit in Figure Q1 (c).

(7 marks)

Q2 (a) A sequence detector consists of a single-input and single-output. This sequence detector will produce an output of '1' if the input sequence detects 101 patterns.

(i) Develop a Moore-type state diagram for the sequence detector.

(3 marks)

(ii) Produce state-assigned table for the detector.

(4 marks)

(iii) Construct the schematic circuitry of sequence detector.

(6 marks)

(b) Consider a stick diagram in Figure Q2 (b).

(i) Produce the electrically equivalent transistor-level.

(4 marks)

(ii) Illustrate the Euler path for transistor level in Q2 (b)(i).

(3 marks)

Q3 (a) Given a function $f(x_1, x_2, x_3, x_4) = \sum m(0,1,3,4,7,11,13,15) + D(9,12,14)$. By using K-Map, produce the minimum-cost SOP function.

(5 marks)

(b) Given a function of f(A,B,C,D) = $\sum$ (0,1,4,5,10,12,14). By using tabular method of simplification:

(i) Construct the First, Second and Third List table.

(9 marks)

(ii) Construct Essential Prime Implicant (EPI) cover table.

(4 marks)

(iii) Produce the minimum cost implementation.

(2 marks)

Q4 (a) For nFET transistor, assume that $k_n^{'}$ = 100x10^{-6}A/V^2, W/L = 0.25μm/0.2μm, V_{DD} = 5V, and V_{TN} = 1V.

(i) Investigate the maximum current flow in the nFET.

(5 marks)

(ii) Decide the aspect ratio needed to obtain a maximum current of 8mA and W = 5μm.

(5 marks)

(b) t_{LH} defines as a time needed for the output arise from the 10%V_{DD} to 90%V_{DD} in digital waveform. Given $t_{LH} = t_{90\%} - t_{10\%}$, where $t_x = \tau_p In\left(\frac{1}{1-\frac{V_x}{V_{DD}}}\right)$, produce the t_{LH} value.

(10 marks)

Q5 (a) Given a simple circuit in Figure Q5(a).

(i) Determine a fault table for the circuit to show the coverage of the various stuck-at-0 and stuck-at-1 faults by the eight possible tests.

(10 marks)

(ii) Predict the minimal test set for this circuit.

(4 marks)

(b) Based on the logic circuit in Figure Q5(b) predict the tests that can detect each of these faults:

(i) $w_2/0$
(ii) $b/1$
(iii) $d/1$

(6 marks)

-END OF QUESTION-

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```
Library ieee;
use ieee.std_logic_1164.all;

entity dec3to8 is
port ( Wa : in std_logic_vector ( 2 downto 0);
       Ena : in std_logic;
        Ya : out std_logic_vector (0 to 7));
end dec3to8;

architecture structural of dec3to8 is
signal s : std_logic_vector (0 to 1);

component dec2to4
port ( w : in std_logic_vector ( 1 downto 0);
     En : in std_logic;
     y : out std_logic_vector(0 to 3));
end component;

Begin
s(0) <= not Wa(2) and Ena;
s(1) <= Wa(2) and Ena;
D1 : dec2to4 port map ( w(1)=>Wa(1), w(0)=>Wa(0), En => s(0), y(0)=>Ya(0),
                        y(1)=> Ya(1),y(2)=> Ya(2),y(3)=> Ya(3));
D2 : dec2to4 port map ( Wa(1 downto 0), s(1), Ya(4 to 7));
End structural;
```

FIGURE Q1(b)

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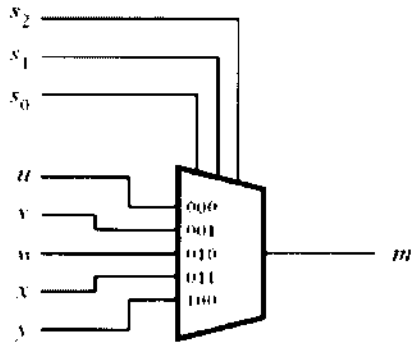

FIGURE Q1(c)

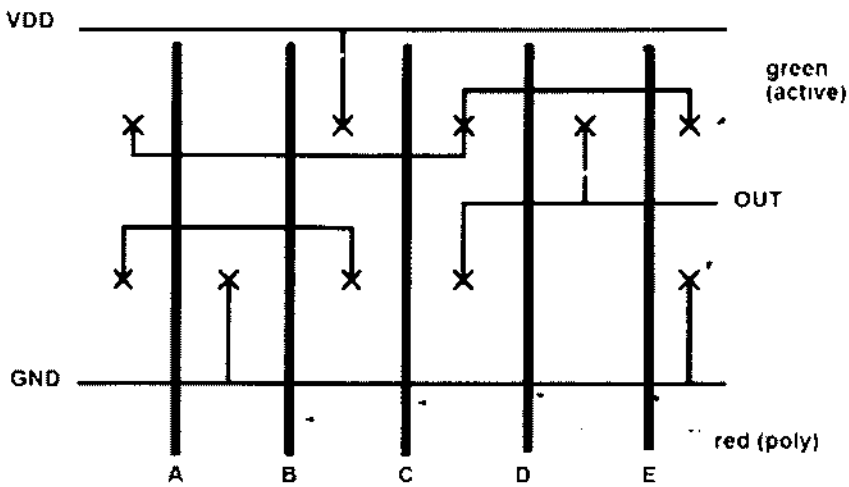

FIGURE Q2(b)

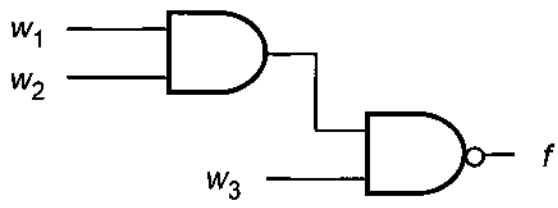

FIGURE Q5(a)

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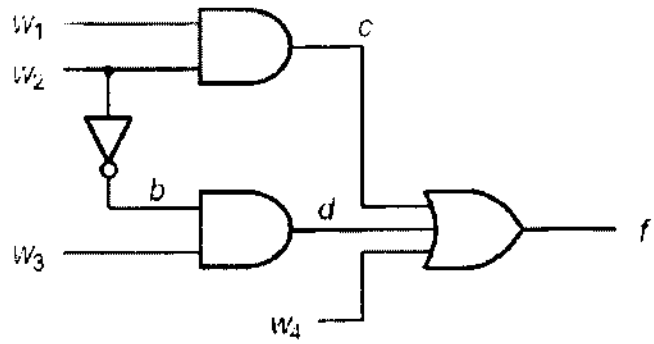

FIGURE Q5(b)