UNIVERSITI TUN HUSSEIN ONN MALAYSIA

FINAL EXAMINATION
SEMESTER II
SESSION 2012/2013

COURSE NAME	:	VLSI DESIGN
COURSE CODE	:	BED 30303
PROGRAMME	:	BED
EXAMINATION DATE	:	JUNE 2013
DURATION	:	2 ½ HOURS
INSTRUCTION	:	ANSWER **FIVE (5)** QUESTIONS ONLY.

THIS QUESTION PAPER CONSISTS OF **SEVEN (7)** PAGES

Q1 For the following function

$$G = \overline{ab + cd + e}$$

(a) Design a static CMOS circuit using minimum number of transistors to realize the function.

(10 marks)

(b) Draw the most compact stick diagram layout for the function.

(10 marks)

Q2 (a) A 2-input multiplexer (2:1 MUX) can be realized by using a pair of transmission gate as shown in **Figure Q2(a)**.

(i) Obtain the equation for output Y of **Figure Q2(a)**.

(2 marks)

(ii) State the advantage of using transmission gate in designing a logic circuit.

(3 marks)

(b) A 4-input multiplexer (4:1 MUX) can be constructed using two 2-input multiplexers as shown in **Figure Q2(b)**. Design the 4-input multiplexer using the transmission gate method. Draw the circuit at transistor level.

(15 marks)

Q3 (a) A Half Adder circuit is shown in gate level in **Figure Q3(a)**. For this circuit:

(i) State the Boolean equations for the output S and C_{out}.

(2 marks)

(ii) Draw the circuit for sum (S) at transistor level using static CMOS.

(8 marks)

(b) A Carry Look-Ahead circuit is usually used along with a Full Adder circuit.

(i) Complete the truth table shown in **Figure Q3(b)** to include two terms Generate (G) and Propagate (P) that is used in the Carry Look-Ahead circuit and obtain the general equation for G and P.

(4 marks)

(ii) Based on the truth table on **Figure Q3(b)**, acquire the equations for S and C_o; and then rewrite the equations S and C_o in term of Generate (G) and Propagate (P) .

(6 marks)

Q4 (a) A Full Adder circuit at transistor level is shown in **Figure Q4(a)**. Acquire the Boolean equations for X, C_o, Y and S

(8 marks)

(b) A block diagram of a 2-to-4 decoder is shown in **Figure Q4(b)**.

(i) Construct the truth table for the decoder and obtain the equation for each output.

(4 marks)

(ii) Design a dynamic 2-to-4 NOR decoder and draw the full circuit at transistor level.

(8 marks)

Q5 (a) In VLSI design, IC designing process can be described in the behavioural, structural and physical domains. Describe these domains.

(6 marks)

(b) Explain the following two most common style of physical clocking networks in VLSI design.

(i) H tree

(3 marks)

(ii) Balanced tree

(3 marks)

(c) One aspect in optimization of VLSI design is in reducing circuit delay. Discuss about RC delay and propose techniques to improve the delay imposed by the resistance of a wire.

(8 marks)

- END OF QUESTION -

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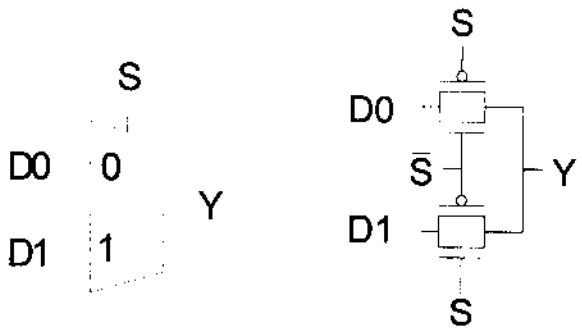

FIGURE Q2(a)

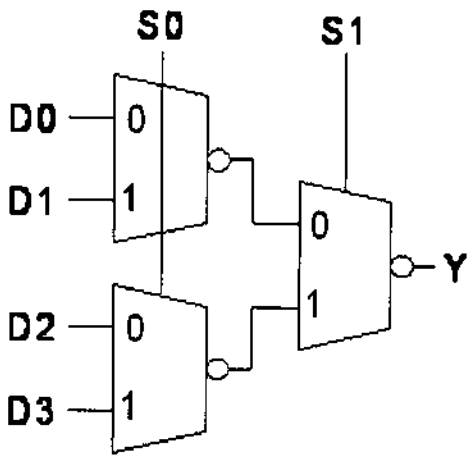

FIGURE Q2(b)

FINAL EXAMINATION

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COURSE : VLSI DESIGN COURSE CODE: BED 30303

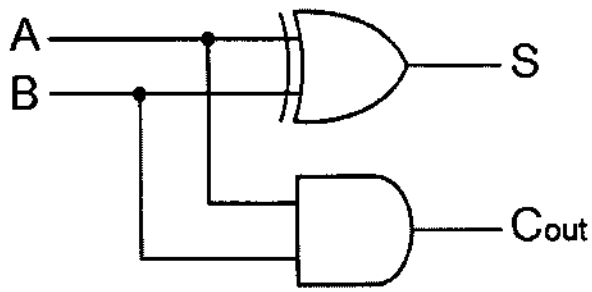

FIGURE Q3(a)

A	B	C_i	S	C_o	P	G
0	0	0	0	0		
0	0	1	1	0		
0	1	0	1	0		
0	1	1	0	1		
1	0	0	1	0		
1	0	1	0	1		
1	1	0	0	1		
1	1	1	1	1		

FIGURE Q3(b)

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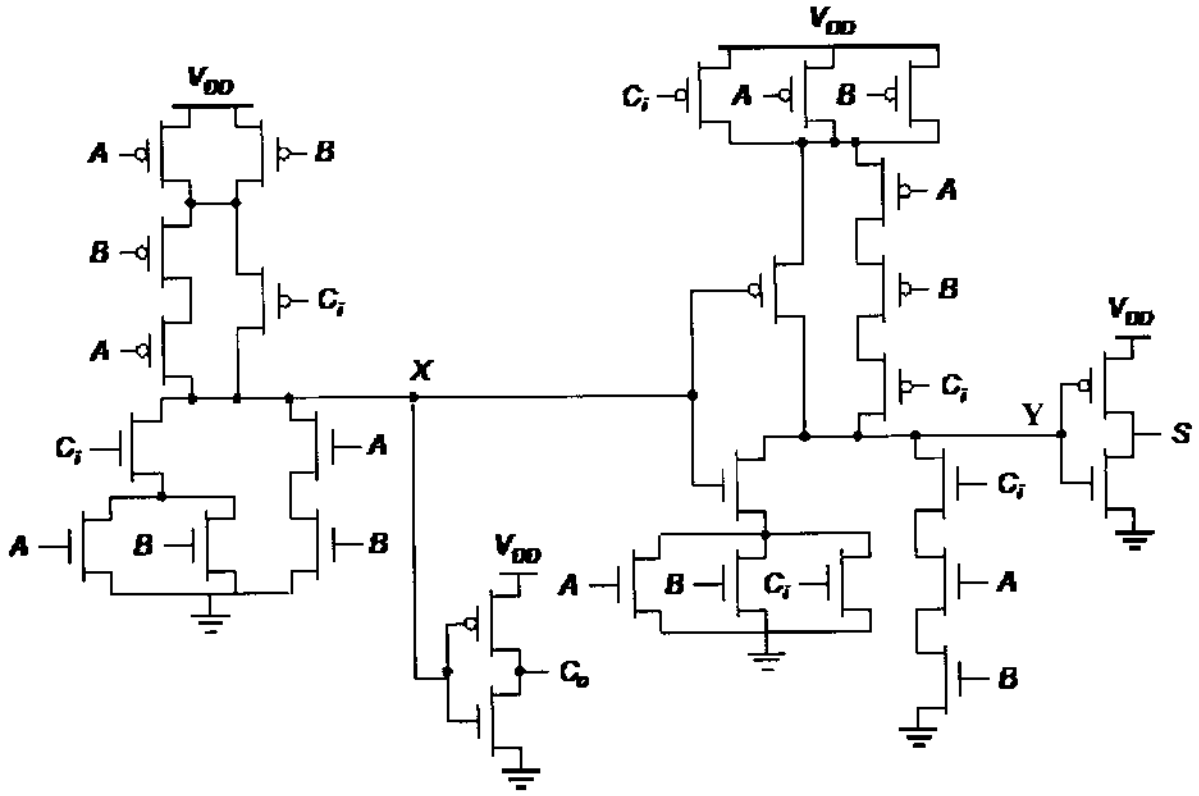

FIGURE Q4(a)

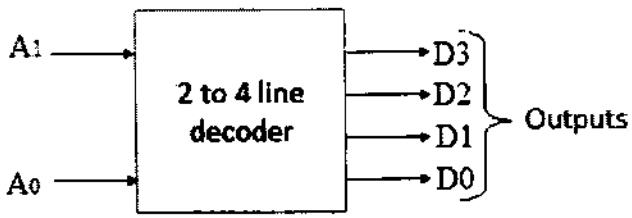

FIGURE Q4(b)