Universiti Tun Hussein Onn Malaysia

UNIVERSITI TUN HUSSEIN ONN MALAYSIA

FINAL EXAMINATION
SEMESTER II
SESSION 2013/2014

COURSE NAME	:	IC PACKAGING
COURSE CODE	:	BED 41103
PROGRAMME	:	4 BEJ
EXAMINATION DATE	:	JUNE 2014
DURATION	:	3 HOURS
INSTRUCTION	:	ANSWER **ALL** QUESTIONS

THIS QUESTION PAPER CONSISTS OF **THREE (3)** PAGES

Q1 (a) Electronic products began shifting from vacuum tubes to the transistors in 1950s and into the integrated circuits (IC) in the 1960s. Continued advances in reducing the size of transistors allowed the progressive integration of tens, hundreds and thousands of on a single IC.

(i) State the definition of IC.

(4 marks)

(ii) Give **TWO (2)** types of IC.

(4 marks)

(iii) Analyze **ALL** integration level of IC technologies.

(5 marks)

(b) Packaging is needed in all IC, which are classified into Through-Hole Technology (THT) and Surface Mount Technology (SMT). Both packages have their own unique packaging process flow.

(i) Compare the mounting difference between THT and SMT.

(6 marks)

(ii) Sketch and explain the flow of IC packaging process flow.

(6 marks)

Q2 (a) Microelectronic packaging was designed to establish interconnections with electrical components such as transistors, diodes, capacitor and resistors to form circuits. It is also needed to ensure the chips and interconnections are packaged in an efficient and reliable manner.

(i) Describe **ALL** packaging levels in microelectronic packaging

(3 marks)

(ii) Based on **Q2(a)(i)**, investigate the package item, function and electrochemical process at every packaging level.

(10 marks)

(b) Chip-package interconnection technologies currently used in semiconductor industry include wire bond and tape automated bonding (TAB). With the aid of a diagram explain in detail of the process below:

(i) Wire Bond

(6 marks)

(ii) Tape automated bond (TAB)

(6 marks)

Q3 (a) In a semiconductor production process, there are two sequential sub-processes commonly referred to front-end process and back-end process. Both of these processes are very important in IC packaging.

(i) Using a diagram, show all the processes involve in the front-end process

(10 marks)

(b) Reliability test is performed on completed packages to assess their ability to survive thermal and moisture-related stresses encountered during actual use condition.

(i) Categorize only **THREE (3)** automated testing processes.

(6 marks)

(ii) Analyze all the inspection done in *In-Process Quality Inspection.*

(9 marks)

Q4 (a) Bonding pads on the entire surface of the chip and the flip-chip connection in ball grid array (BGA) package are expected to produce good results of size reduction.

(i) Design a diagram showing the flip-chip interconnection.

(5 marks)

(ii) Analyze **ALL** flip-chip bonding processes.

(10 marks)

(iii) Design the flip-chip assembly process.

(5 marks)

(iv) State the advantages of flip-chip interconnection.

(5 marks)

- END OF QUESTION -