Universiti Tun Hussein Onn Malaysia

UNIVERSITI TUN HUSSEIN ONN MALAYSIA

FINAL EXAMINATION
SEMESTER II
SESSION 2013/14

COURSE NAME	:	DIGITAL SYSTEMS DESIGN
COURSE CODE	:	BEX31503
PROGRAMME	:	BEE
EXAMINATION DATE	:	JUNE 2014
DURATION	:	3 HOURS
INSTRUCTIONS	:	ANSWER **ALL** QUESTIONS

THIS QUESTION PAPER CONSISTS OF **FIVE (5)** PAGES

Q1 In the context of field programmable gate array (FPGA) design flow, briefly explain the following concept.

(a) Design entry

(2 marks)

(b) Functional simulation

(2 marks)

(c) Timing simulation

(2 marks)

Q2 (a) Complete the spectrum of possible hardware solution and the trade-offs of different implementation approaches as shown in Table **Q2**.

TABLE Q2

Platform	Performance	Cost	Power	Flexibility	Design Effort
ASIC	(3)	High	Low	Low	High
DSP	Medium	Medium	Medium	Medium	(6)
(1)	Low	Low	(4)	High	Low
(2)	High	Medium	High	Medium	Medium
RH	Medium/High*	Medium	High/Low#	(5)	Medium

Note:
* Depends on technology and available embedded resources
\# With Xilinx Spartan's FPGA

(7 marks)

(b) Suggest the most suitable platform for numerous data-intensive applications that can offer high-throughput with critical time constraints. Then, give justification to support your suggestion.

(7 marks)

Q3 Write a VHDL and Verilog code for the Boolean function in Equation (1).

$$f = x1 \cdot x2 + \overline{x2} \cdot x3 \qquad \ldots\ldots\ldots \quad (1)$$

(6 marks)

Q4 Figure **Q4** shows the simulation results for "X" circuit with six (6) inputs and two (2) outputs.

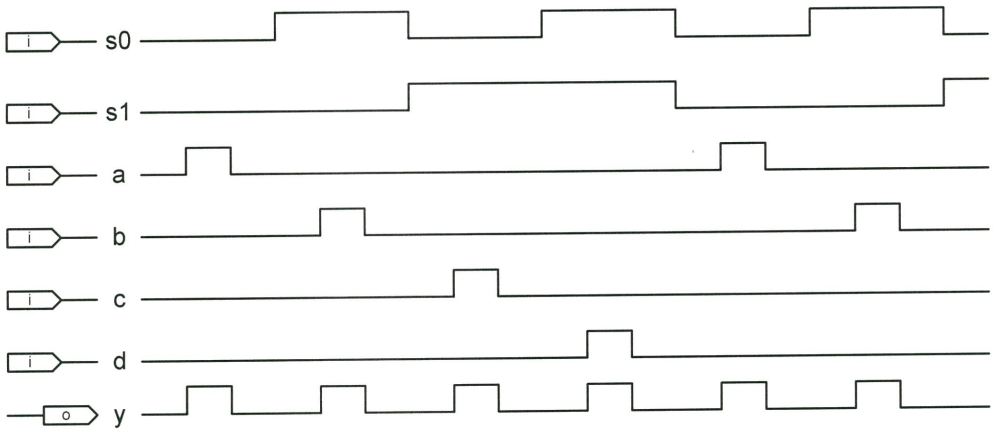

FIGURE Q4

(a) What is the function of "X" circuit?

(2 marks)

(b) With concurrent statements of WHEN/ELSE, write a complete VHDL code that will give the simulation results as shown in Figure **Q4**.

(8 marks)

Q5 (a) In VHDL programming, differentiate between library, entity and architecture.

(6 marks)

(b) What are the rules of valid entity name in VHDL?

(4 marks)

(c) You are required to implement curvelet transform algorithm on the Virtex UltraScale device. List any relevant design parameters as a performance measurement.

(5 marks)

Q6 Carry-ripple and carry-lookahead are two (2) classical approaches to the design of adders. The former has the advantage of requiring less hardware, whilst the latter is faster.

You are required to design an 8-bit carry-ripple adder with its outputs can be computed by means of the following expressions.

$$s_j = a_j \text{ XOR } b_j \text{ XOR } c_j \quad \ldots\ldots\ldots (2)$$

$$c_{j+1} = (a_j \text{ AND } b_j) \text{ OR } (a_j \text{ AND } c_j) \text{ OR } (b_j \text{ AND } c_j) \quad \ldots\ldots\ldots (3)$$

(a) Propose the top-level diagram for your carry-ripple adder.

(2 marks)

(b) Based on your top-level diagram, suggest the one-level below top diagram your design.

(5 marks)

(c) With the concept of logic vectors data type, write a complete VHDL code to implement your design.

(13 marks)

Q7 The sketch of a 2-bit comparator testbench setup is shown in Figure **Q7**.

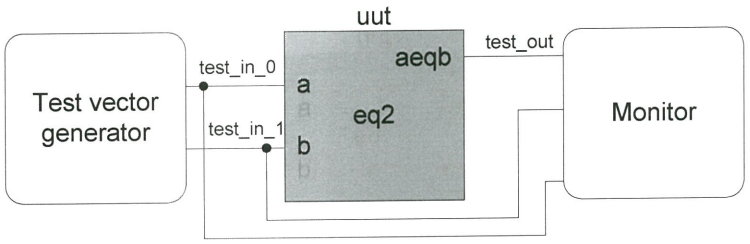

FIGURE Q7

(a) In brief, explain the testbench setup shown in Figure **Q7**.

(2 marks)

(b) Suggest a complete VHDL code testbench for the unit under test (uut).

(10 marks)

Q8 Multiplication followed by accumulation is a common operation in many digital systems, particularly those highly interconnected, like digital filters, neural networks and data quantizers. A typical multiply-accumulate (MAC) architecture is illustrated in Figure **Q8**. It consists of multiplying two (2) values, then adding the result to the previously accumulated value, which must then be re-stored in the registers for future accumulations.

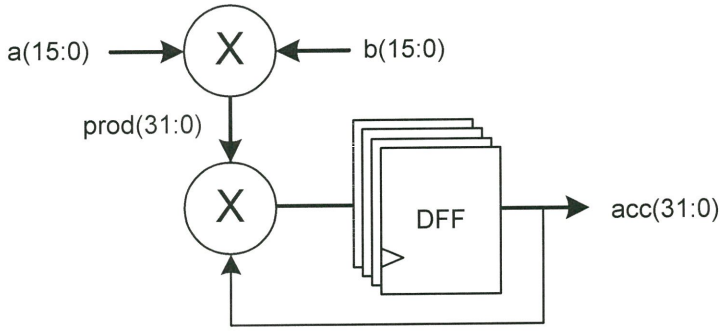

FIGURE Q8

(a) With the concept of FUNCTIONS, write a complete VHDL code as a package to be used in any future design.

(7 marks)

(b) To utilise the package that has been designed in (a), write a complete VHDL code to implement a MAC circuit shown in Figure **Q8**.

(10 marks)

- END OF QUESTIONS -