Universiti Tun Hussein Onn Malaysia

UNIVERSITI TUN HUSSEIN ONN MALAYSIA

FINAL EXAMINATION
SEMESTER I
SESSION 2013/2014

COURSE NAME	:	DIGITAL DESIGN
COURSE CODE	:	BEC 30503
PROGRAMME	:	BEJ
EXAMINATION DATE	:	JANUARY 2014
DURATION	:	3 HOURS
INSTRUCTION	:	ANSWER **ALL** QUESTIONS

THIS QUESTION PAPER CONSISTS OF **SEVEN (7)** PAGES

Q1 In the context of digital design and computer arithmetic, briefly explain the following concept.
Note: Use an appropriate diagram to support your explanation.

(a) Parallel data transmission

(2 marks)

(b) Moore machines

(2 marks)

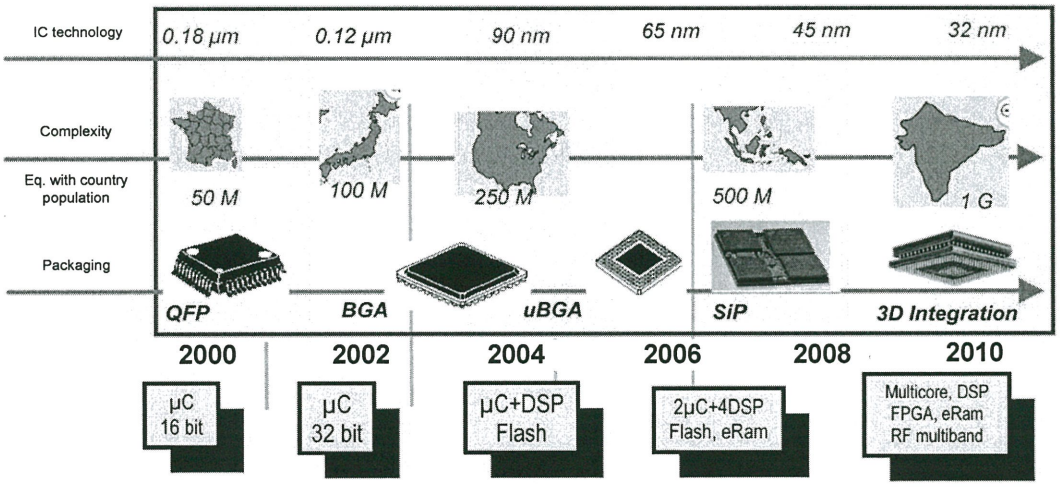
(c) Pipelining and parallelism

(2 marks)

(d) Design entry

(2 marks)

Q2 The trend of complementary metal oxide semiconductor (CMOS) technology improvement continues to be driven by the need to integrate more functions within a given silicon area as depicted in Figure **Q2**. As an example, the 32-nm CMOS technology enables designs with multi-core processors, parallel digital signal processors (DSPs), field programmable gate arrays (FPGAs), embedded random access memory (eRAM), as well as wireless communication capabilities in a single chip. Discuss two (2) points of view related with the trend shown as well as the validity of Moore's law that has been outlined in 1965.



Source:
S. M. Aziz, E. Sicard, and S. B. Dhia, Effective Teaching of the Physical Design of Integrated Circuits using Educational Tools, *IEEE Transactions on Education*, Vol. 53, No. 4, November 2010, pp. 517 - 531

FIGURE Q2

(4 marks)

Q3 In your circuit design, two (2) major problems have been identified: high power consumption and interconnect delay. As project leader for a group of an application specific integrated circuit (ASIC) engineer, recommend solutions to solve these problems.

(2 marks)

Q4 Based on the design specification given in Figure **Q4**, write two (2) conclusions that can be made to relate with the very large scale integration (VLSI) designer philosophy.

- Technology: 0.8 μm twin-well CMOS
- Propagation delay signals < 1.2ns
- Transition times < 1.2 ns
- Circuit area < 1500 μm^2
- Dynamic power dissipation < 1mW

FIGURE Q4

(2 marks)

Q5 Answer TRUE or FALSE.

(a) All VHDL files require an entity declaration and an architecture body.

(1 mark)

(b) The architecture body indicates the input and output ports of the VHDL design.

(1 mark)

(c) A port in VHDL is a connection from a VHDL design entity to the outside world.

(1 mark)

(d) The VHDL language was originally developed by the Institute of Electrical Engineers (IEE) committee as a standardised language for describing hardware.

(1 mark)

(e) `FKEE_boleh` is a valid name for any entity in a VHDL design.

(1 mark)

Q6 Verify the VHDL code shown in Figure **Q6** and suggest the solution to fix all these errors.

```
1   LIBRARY ieee;
2   USE ieee.std_logic_1164.all
3   ENTITY component IS
4   PORT (   w, x, y, z   :  IN     STD_LOGIC;
5            f            :  OUT    STD_LOGIC_VECTOR);
6   END component;
7   ARCHITECTURE mycircuit IS
8   BEGIN
9   f <= (w AND x) OR (y AND z);
10  END architecture mycircuit;
```

FIGURE Q6

(8 marks)

Q7 Write a VHDL code for the circuit of Figure **Q7**.

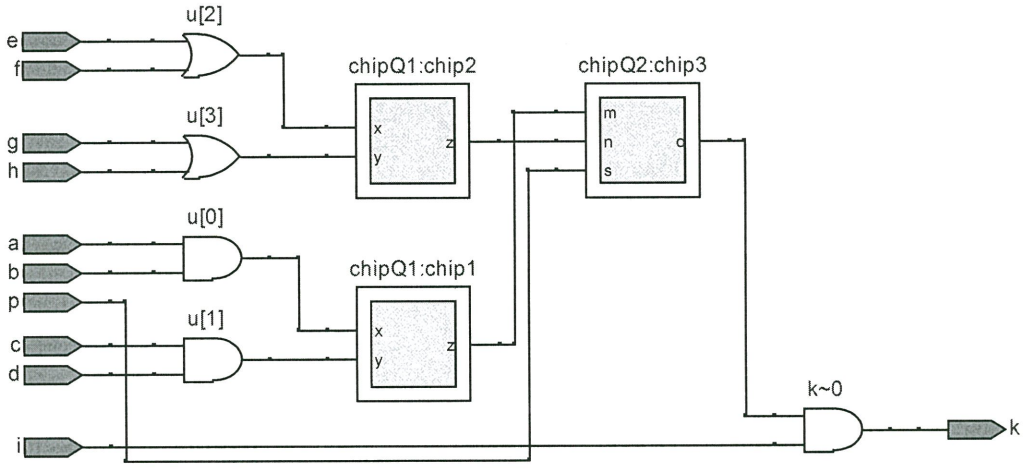


FIGURE Q7

(10 marks)

Q8 Figure **Q8** shows a top-level diagram of a signed comparator. The size of the vectors to be compared is generic ($n + 1$).

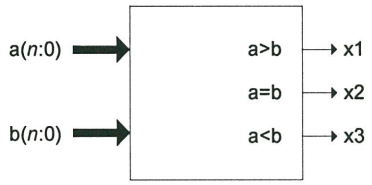


FIGURE Q8

(a) Write the library declarations

(2 marks)

(b) Write the entity section for the signed comparator to be implemented.

(4 marks)

(c) List all lines required in the architecture section of the VHDL code.

(5 marks)

Q9 We want to calculate $y = a/b$, where a, b, and y have the same number ($b + 1$) bits. The algorithm is illustrated in Table **Q9** for a = "1011" (decimal 11) and b = "0011" (decimal 3), whilst the results of y = "0011" (decimal 3) and remainder "0010" (decimal 2).

TABLE Q9

Index (i)	a-related input (a_inp)	Comparison	b-related input (b_inp)	y (quotient)	Operation on the 1st column
3	1011	<	0011000	0	none
2	1011	<	0001100	0	None
1	1011	>	0000110	1	a_inp(i) – b_inp(i)
0	0101	>	0000011	1	a_inp(i) – b_inp(i)
	0010 (rem)				

(a) In five (5) sentences, elaborate about the processes involved in the algorithm.

(10 marks)

(b) To realise the algorithm in Table **Q9**, both IF and LOOP plus IF statements are possible to be employed.

(i) Conclude and justify the best statement to be used.

(3 marks)

(ii) Develop a VHDL code for the division algorithm.

(15 marks)

Q10 Digital signal processing (DSP) find innumerable applications and are generally based on linear time invariant (LTI) that can be represented as:

$$\sum_{k=0}^{N} a_k y[n-k] = \sum_{k=0}^{M} b_k x[n-k] \quad \ldots\ldots\ldots \quad (1)$$

where a_k and b_k are the filters coefficients, and $x[n-k]$, $y[n-k]$ are the current (for $k=0$) and earlier (for $k>0$) input and output values, respectively. The impulse response of a digital filter can be divided into two categories: infinite impulse response (IIR) and finite impulse response (FIR) and only FIR filters can exhibit linear phase, so they are indispensable when linear phase is required, like in many telecommunication applications. With $N=0$, Equation (1) becomes

$$y[n] = \sum_{k=0}^{M} c_k x[n-k] \quad \ldots\ldots\ldots \quad (2)$$

where $c_k = b_k / a_0$ are the coefficients of the FIR filter.

(a) With four (4) coefficients, sketch the FIR filter diagram.

(3 marks)

(b) Sketch an equivalent register transfer level (RTL) representation of the FIR filter.

(3 marks)

(c) To execute the FIR filter using HDL-based design entry, functional and timing simulations are required. Differentiate between these two (2) simulations.

(4 marks)

(d) To prototype the design, field programmable gate array (FPGA)-based implementation will be carried out. List five (5) parameters to be used as a performance measurement in your design.

(5 marks)

(e) Complete the VHDL code shown in Figure **Q10**.

(7 marks)

```
1   ------------------------------------------
2   LIBRARY ieee;
3   USE ieee.std_logic_1164.all;
4   USE ieee.std_logic_arith.all;
5   ------------------------------------------
6   ENTITY Q10e IS
7      (1)____ (n: INTEGER := 4; m: INTEGER := 4);
8      PORT ( x: IN SIGNED (m-1 DOWNTO 0);
9             clk, rst: IN (2)____;
10            y: OUT SIGNED (2*m-1 DOWNTO 0));
11  END Q10e;
12  ARCHITECTURE rtl OF Q10e IS
13     TYPE registers IS (3)____ (n-2 DOWNTO 0) OF SIGNED (m-1 DOWNTO 0);
14     TYPE coefficients IS ARRAY (n-1 DOWNTO 0) OF SIGNED (m-1 DOWNTO 0);
15     (4)____ reg: registers;
16     CONSTANT coef: coefficients := ("0001", "0010", "0011", "0100");
17  BEGIN
18     (5)____ (clk, rst)
19         VARIABLE acc, prod:
20              SIGNED(2*m-1 DOWNTO 0) := (OTHERS=>'0');
21         VARIABLE sign: STD_LOGIC;
22     BEGIN
23  ------reset-----------------------------------------
24         IF (rst='1') THEN
25              FOR i IN n-2 DOWNTO 0 LOOP
26                FOR j IN M-2 DOWNTO 0 LOOP
27                     reg(i)(j)<='0';
28                END LOOP;
29              END LOOP;
30  ------register inference + MAC:--------------------
31         ELSEIF (clk'EVENT AND clk='1') THEN
32              acc := coef(0)*x;
33              FOR i IN 1 (6)____ n-1 LOOP
34                sign := acc(2*m-1);
35                prod := coef(i)reg(n-1-i);
36                acc := acc + prod;
37  ------overflow check ------------------------------
38                IF (sign = prod(prod'left)) AND (acc(acc' := acc + prod;
39                       THEN
40                       acc := (acc'LEFT => sign, OTHERS => NOT sign;
41                END IF;
42              END LOOP;
43              reg <= x & reg (n-2 DOWNTO 1);
44         END IF;
45         y <= acc;
46     END (7)____;
47  END rtl;
```

FIGURE Q10

- END OF QUESTIONS -