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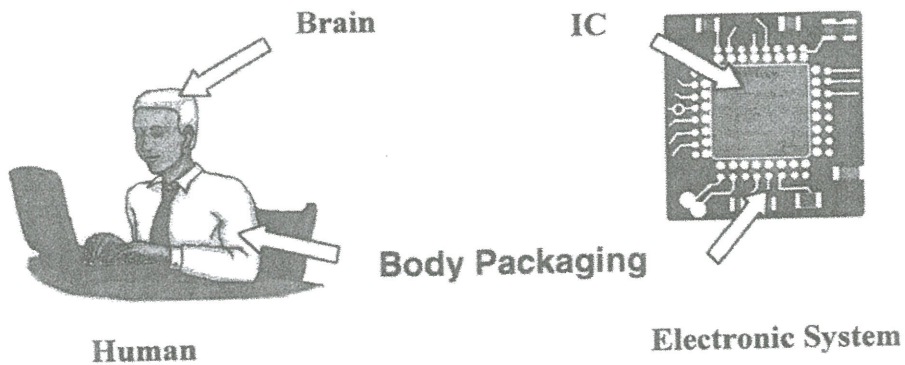
**FINAL EXAMINATION  
SEMESTER I  
SESSION 2014/2015**

COURSE NAME : IC PACKAGING  
COURSE CODE : BED 41103  
PROGRAMME : 4 BEJ  
EXAMINATION DATE : DECEMBER 2014 / JANUARY 2015  
DURATION : 3 HOURS  
INSTRUCTION : ANSWER ALL QUESTIONS

THIS QUESTION PAPER CONSISTS OF **FOUR (4)** PAGES

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- Q1** (a) Electronics devices such as mobile phone, computer and microwave oven are based on Microsystem Technologies.
- (i) Define Microsystems? (4 marks)
  - (ii) List **FOUR** Microsystems Products. (4 marks)
  - (iii) Give **FOUR** evolution waves in Microsystems Technologies. (4 marks)
- (b) The electronic product is like a human body. The brain and body parts are related with each other.
- (i) Match **FOUR** analogies between human body and electronic packaging as shown in **FIGURE Q1(b)**. (4 marks)
  - (ii) Explain the relation between Information Technology (IT), Microsystems and Packaging. (4 marks)



**FIGURE Q1(b)**

- Q2** (a) Electronic products began shifting from vacuum tubes to the transistors in 1950s and into the integrated circuits (IC) in the 1960s. Continued advances in reducing the size of transistors allowed the progressive integration of tens, hundreds and thousands of on a single IC.
- (i) State the definition of IC. (2 marks)
  - (ii) Give **TWO** types of IC. (4 marks)

- (iii) Analyze **ALL** integration level of IC technologies. (4 marks)
- (b) Packaging is needed in all IC, which are classified into Through-Hole Technology (THT) and Surface Mount Technology (SMT). Both packages have their own unique packaging process flow.
- (i) Compare the mounting difference between THT and SMT. (5 marks)
- (ii) Define Ball Grid Array (BGA) (2 marks)
- (iii) Draw a diagram of BGA building-up. (3 marks)
- Q3** (a) Microelectronic packaging was designed to establish interconnections with electrical components such as transistors, diodes, capacitor and resistors to form circuits. It is also needed to ensure the chips and interconnections are packaged in an efficient and reliable manner.
- (i) Classify **ALL** packaging levels in microelectronic packaging (4 marks)
- (ii) Describe the package item, function and electrochemical process at every packaging level. (6 marks)
- (b) Chip-package interconnection technologies currently used in semiconductor industry include wire bond and tape automated bonding (TAB). With the aid of a diagram explain in detail the interconnection technique and give three advantages of this technique:
- (i) Explain clearly the Wire Bond technique and give **THREE** advantages (5 marks)
- (ii) Describe in detail the Tape automated bond (TAB) technique and give **THREE** advantages (5 marks)

- Q4** (a) Failure mechanisms in an electronic product are several. They are caused by thermo-mechanical, electrical, chemical and environmental mechanisms.
- (i) Analyse **FIVE** thermomechanical fundamentals. (10 marks)
- (b) The symptoms of failure in electronic devices are always observed at the system level. Understanding the mechanism that cause components failure are the key to make reliable microelectronic package.
- (i) Classify **THREE** failure mechanisms. (3 marks)
- (ii) Explain in detail the failure mechanisms in part **Q4(b)(i)**. (7 marks)
- Q5** (a) Bonding pads on the entire surface of the chip and the flip-chip connection in ball grid array (BGA) package are expected to produce good results of size reduction.
- (i) Design a diagram showing the flip-chip interconnection. (4 marks)
- (ii) Analyze **ALL** flip-chip bonding processes. (8 marks)
- (iii) Design the flip-chip assembly process. (4 marks)
- (iv) State the advantages of flip-chip interconnection. (4 marks)

- END OF QUESTION -