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UNIVERSITI TUN HUSSEIN ONN MALAYSIA

FINAL EXAMINATION
SEMESTER II
SESSION 2015/2016

COURSE NAME	:	DIGITAL ELECTRONICS
COURSE CODE	:	BEL 20303
PROGRAMME	:	BEJ / BEV
EXAMINATION DATE	:	JUNE / JULY 2016
DURATION	:	3 HOURS
INSTRUCTION	:	1. ANSWER **ALL** QUESTIONS 2. ATTACH **APPENDIX A & C** WITH YOUR ANSWER BOOKLET.

THIS QUESTION PAPER CONSISTS OF **TEN (10)** PAGES

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Q1 (a) Explain **THREE (3)** types of signed number representation used in binary numbering system.

(6 marks)

(b) Assuming that all numbers can be represented using 8-bit binary, complete the missing entries which are not shaded in the Table 1. Also assume two's complement numbering system is used when necessary. (No mark will be given for this question unless all the solutions are shown).

(8 marks)

Table 1 : Set numbers in numerical representation

	Binary	Hexadecimal	Unsigned Decimal	Signed Decimal	Gray
Set number 1	?		81		?
Set number 2		D4	?	?	

(c) Simplify the following expressions using Boolean algebra.

(i) $\overline{AB + AC} + \overline{A}\overline{B}C$

(3 marks)

(ii) $(A + C)(A + \bar{B})$

(3 marks)

Q2 (a) Table 2 shows a truth table of a four-input and two-output logic function. Use Karnaugh maps and derive:

(i) the minimal sum-of-product (MSOP) of expression for Y

(4 marks)

(ii) the minimal product-of-sum (MPOS) of expression for Z

(4 marks)

Table 2 : Truth table of a four-input and two-output logic function.

INPUT				OUTPUT	
A	B	C	D	Y	Z
0	0	0	0	1	1
0	0	0	1	0	0
0	0	1	0	0	1
0	0	1	1	0	0
0	1	0	0	1	0
0	1	0	1	X	0
0	1	1	0	1	0
0	1	1	1	0	0
1	0	0	0	0	X
1	0	0	1	X	0
1	0	1	0	X	1
1	0	1	1	1	0
1	1	0	0	1	1
1	1	0	1	1	X
1	1	1	0	X	0
1	1	1	1	X	1

(b) Given the Boolean expression

$$Z = \overline{PQ(RS + \bar{P}S)(\overline{PQ} + \overline{RS})}$$

(i) Simplify expression Z using Boolean theorem.

(6 marks)

(ii) Implement the function Z in part **Q2(b)(i)** using only a 2-input NAND gates.

(6 marks)

Q3 (a) **Figure Q3(a)(i)** shows a logic circuit that comprises of a JK, SC and D flip-flop. **Figure Q3(a)(ii)** shows the waveforms for signal CLK, X, Y, $\overline{CLR}$ and $\overline{PRE}$. Complete the timing diagram for Q_A, Q_B and Q_C in **APPENDIX A**. Assume that Q_A, Q_B and Q_C are at high level initially.

(10 marks)

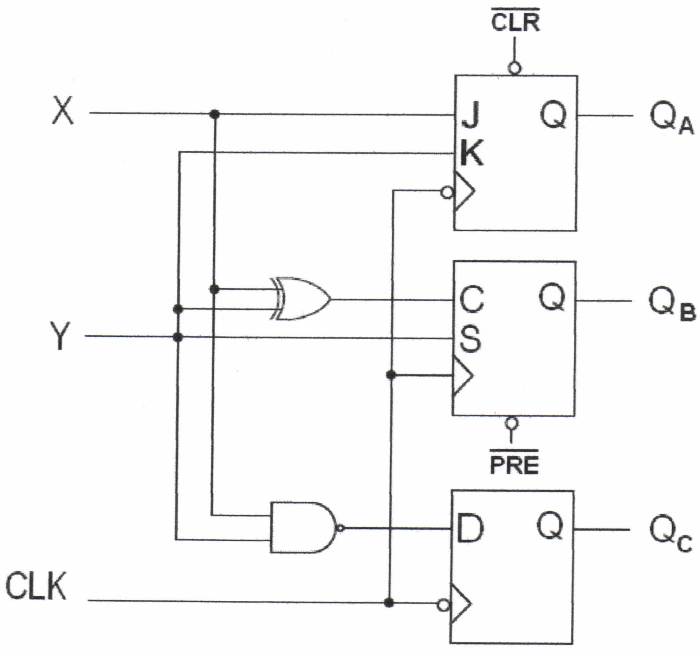

Figure Q3(a)(i)

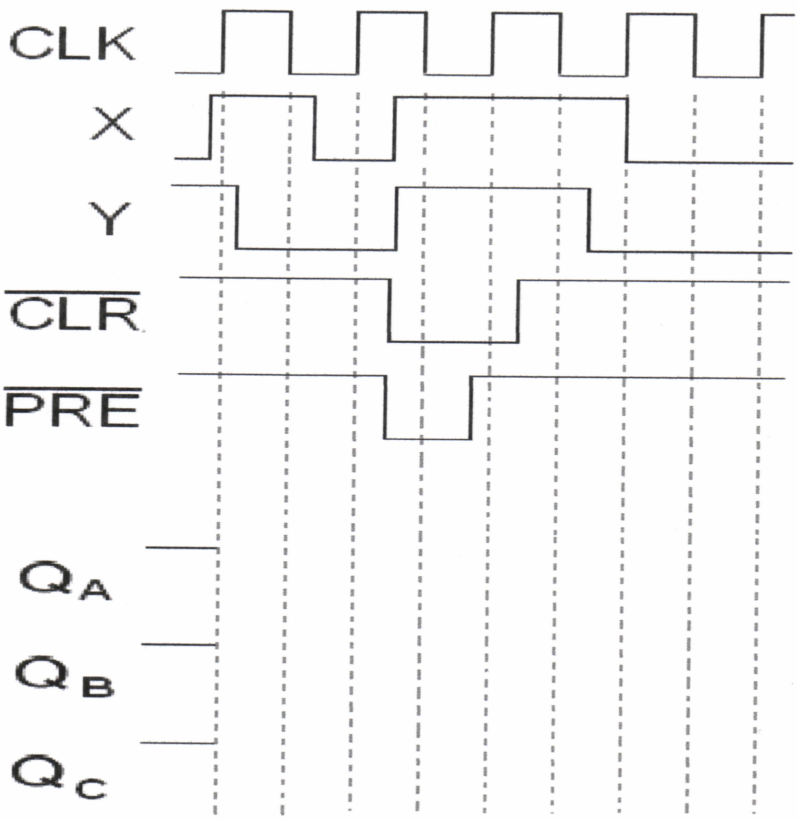

Figure Q3(a)(ii)

(b) **Figure Q3(b)** shows four switches that are part of a control circuitry in a copy machine. The switches are at various points along the path of the copy paper as the paper passes through the machine. Each switch is normally open and as the paper passes over a switch, the switch closes. It is impossible for switches SW1 and SW4 to be closed at the same time (they are far apart and the paper cannot cover them at the same time). Design the logic circuit to produce a HIGH output whenever two or more switches are closed at the same time. Use K mapping and take advantages of the don't-care conditions. Note that the switch will be HIGH when it closes.

(10 marks)

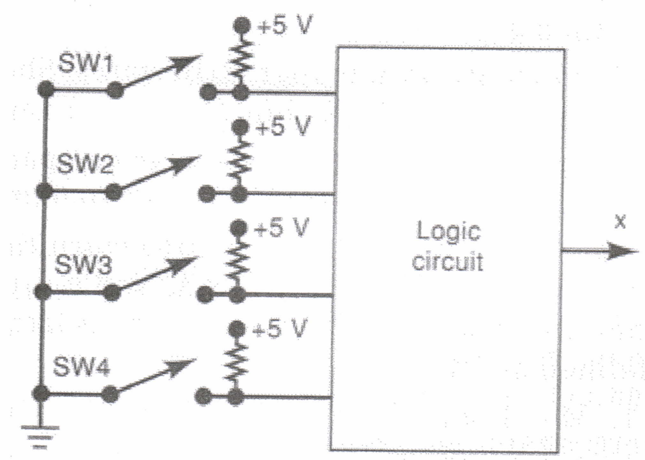

Figure Q3(b)

Q4 (a) Circuit in **Figure Q4(a)** has three inputs (A, B and C) and one output (Z). Construct the truth table for the circuit. Refer to **APPENDIX B** to know the pin assignment of SN7400N.

(10 marks)

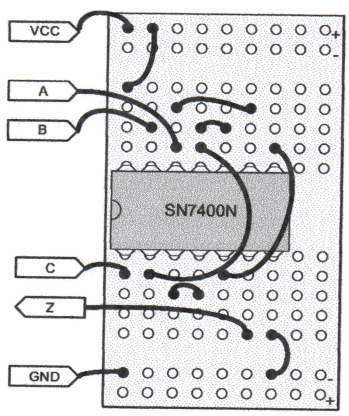

Figure Q4(a)

(b) **Figure Q4(b)** shows a multiplexer 74LS151 (8 line-to-1 line multiplexer). Based on the truth table obtained in part **Q4(a)**, implement the circuit of function Z using 74LS151 multiplexer. Show all connections and please answer in **APPENDIX C**.

(10 marks)

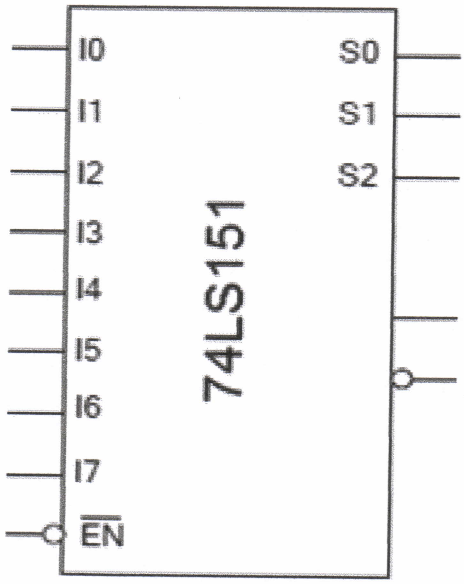

Figure Q4(b)

Q5 **Figure Q5** shows the state transition diagram of a state machine.

(i) Build the excitation table for this state machine. Use JK flip-flops.

(10 marks)

(ii) Find the simplest Boolean expression for the circuit using Karnaugh map.

(6 marks)

(iii) Draw the circuit.

(4 marks)

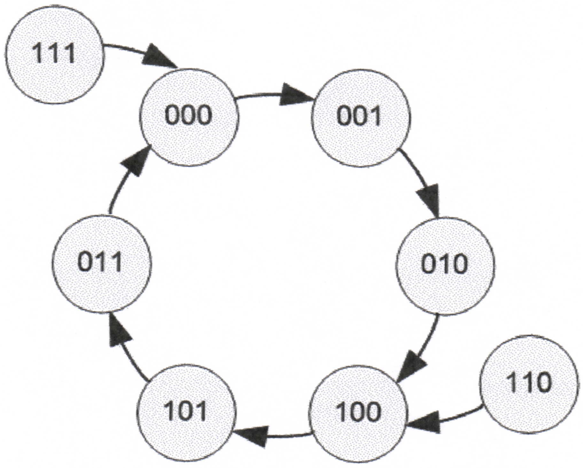

Figure Q5

- END OF QUESTIONS -

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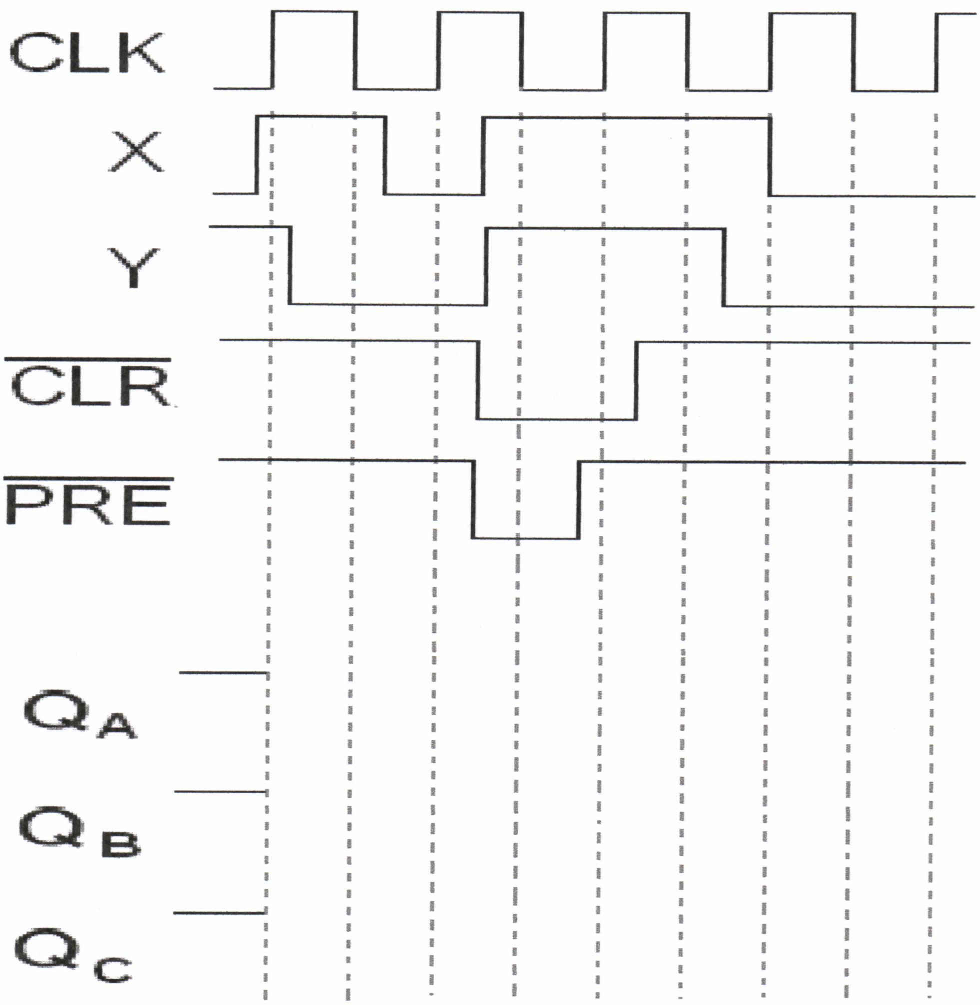
APPENDIX A



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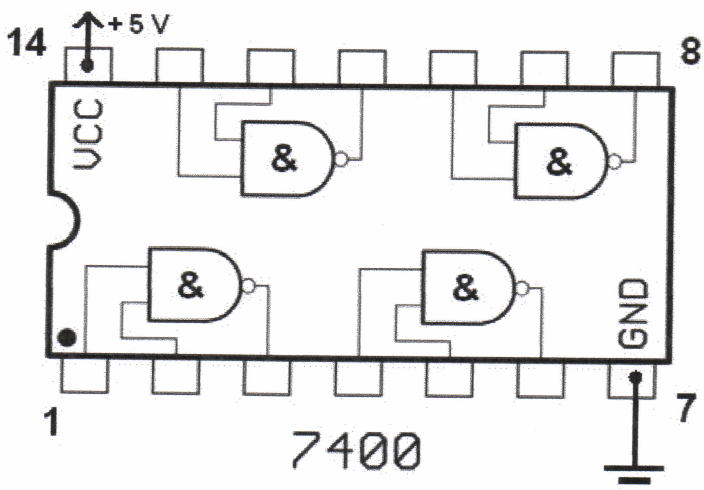
APPENDIX B

PIN ASSIGNMENT AND INTERNAL CIRCUITRY

SN7400N (NAND Gate)



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APPENDIX C