Universiti Tun Hussein Onn Malaysia

UNIVERSITI TUN HUSSEIN ONN MALAYSIA

FINAL EXAMINATION
SEMESTER II
SESSION 2015/2016

COURSE NAME	:	DIGITAL TECHNIQUES
COURSE CODE	:	BEF12302
PROGRAMME	:	BEV
EXAMINATION DATE	:	JUNE / JULY 2016
DURATION	:	2 HOURS
INSTRUCTION	:	1. ANSWER **ALL** QUESTIONS
		2. ATTACH **APPENDIX A, B AND C** WITH YOUR ANSWER BOOKLET

THIS QUESTION PAPER CONSISTS OF **NINE (9)** PAGES

Q1 (a) List five advantages of digital data as compared to analogue data.

(5 marks)

(b) Convert the hexadecimal number A2E6 to BCD code.

(6 marks)

(c) Convert the Gray code 111011000110 to octal number.

(6 marks)

(d) Prove that Boolean expression for Z in **Figure Q1(d)** is equal to $B\overline{D}$ by using Boolean Theorem.

(8 marks)

Q2 (a) Given the Boolean expression

$$Z = \overline{A \cdot B} + A \cdot B \cdot C \cdot D + (A \oplus C)$$

(i) Simplify the Boolean expression using Boolean Theorem.

(5 marks)

(ii) Simplify the Boolean expression using K-Map approach with minimum Sum of Product expression.

(6 marks)

(iii) Draw the combinational logic circuit for Z.

(3 marks)

(b) Manipulate and draw the equation below into NAND gate using Boolean algebra.

$$Z = (\overline{A}.B) + (C.\overline{D})$$

(5 marks)

(c) Find the minimum products of sum for the following function by implementing K-Map:

$$f(a,b,c,d) = \sum m(1,3,4,11) + \sum d(2,7,8,12,14,15)$$

(6 marks)

Q3 (a) Explain the operation of the following functional combinational logic circuit. You may use appropriate diagram to aid your explanation.

i) Multiplexers.

(2 marks)

ii) Comparators

(2 marks)

(b) Implement the following Boolean function using 4-to-1 line multiplexer in **APPENDIX A**.

$$f(w,x,y,z) = \sum m(2,3,5,6,7,9,13,14)$$

(10 marks)

(c) Implement the following Boolean expression using IC 74LS138 (3-to-8 decoder) in **APPENDIX B**. Symbol for IC 74LS138 is shown in **APPENDIX B** for the internal circuitry and pins assignment of 74LS138 (3-to-8 decoder).

$$Z = \overline{(A.B)} + \overline{(B+C)}$$

(8 marks)

(d) Explain the different between synchronous and asynchronous system in sequential circuit.

(3 marks)

Q4 (a) **Figure Q4(a)(i)** shows a logic circuit that comprises of a JK flip-flop, an OR gate and an inverter. **Figure Q4(b)(ii)** shows the waveforms for signal CLK, J, K, $\overline{PRE}$ and $\overline{CLR}$. Complete the timing diagram for Q in **APPENDIX C** and write down the operation (e.g. HOLD) that takes place in each clock pulse as illustrated in the diagram.

(7 marks)

(b) Design a 3-bit synchronous counter which counts in the sequence, 001, 011, 010, 110, 111, 101, 100, (repeat) 001. Draw the combinational circuit using D flip-flops.

(10 marks)

(c) Point out the two model and briefly compare the two types of the state machine.

(6 marks)

(d) Explain the operation of the Serial In Serial Out (SISO) register.

(2 marks)

-END OF QUESTION-

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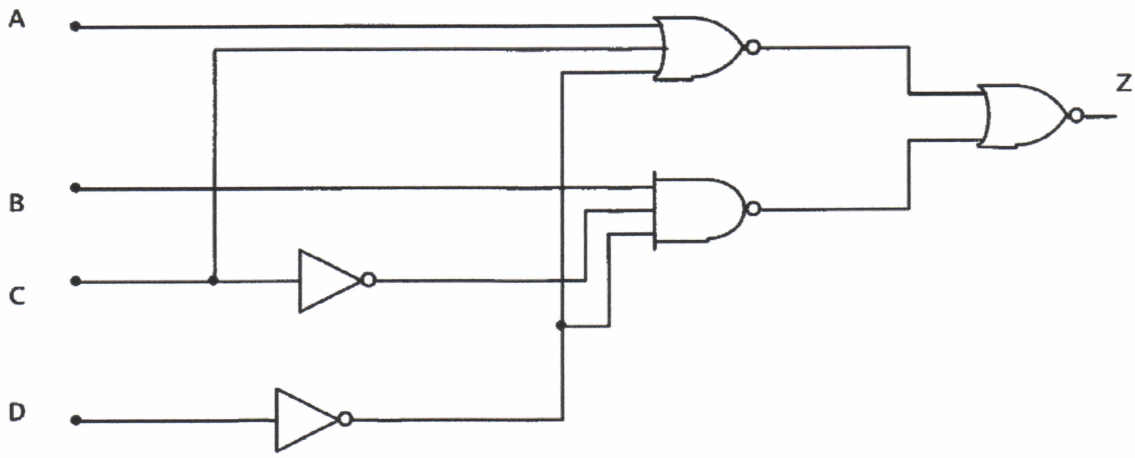

FIGURE Q1(d)

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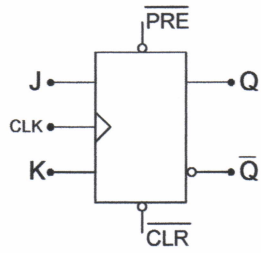

FIGURE Q4(a)(i)

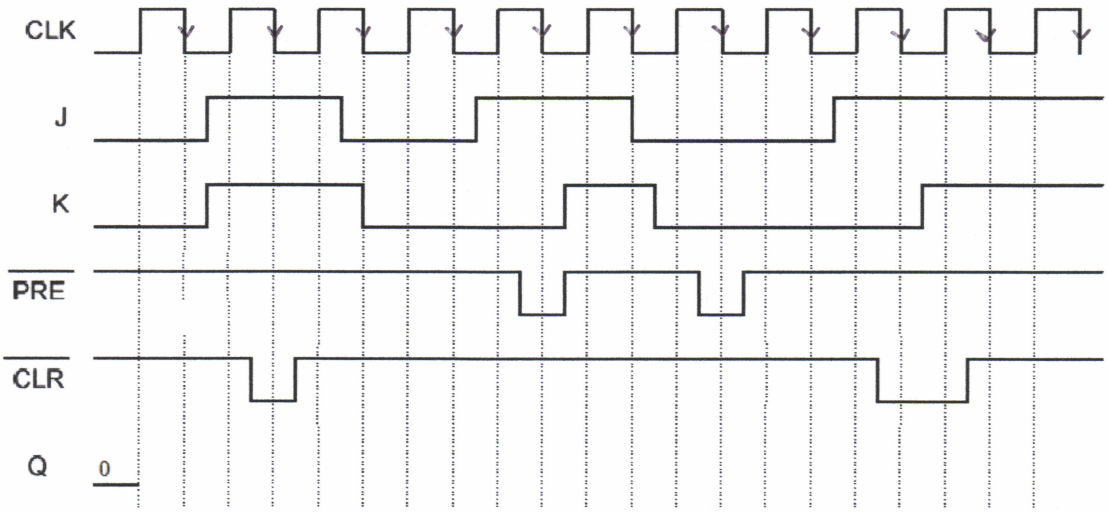

FIGURE Q4(a)(ii)

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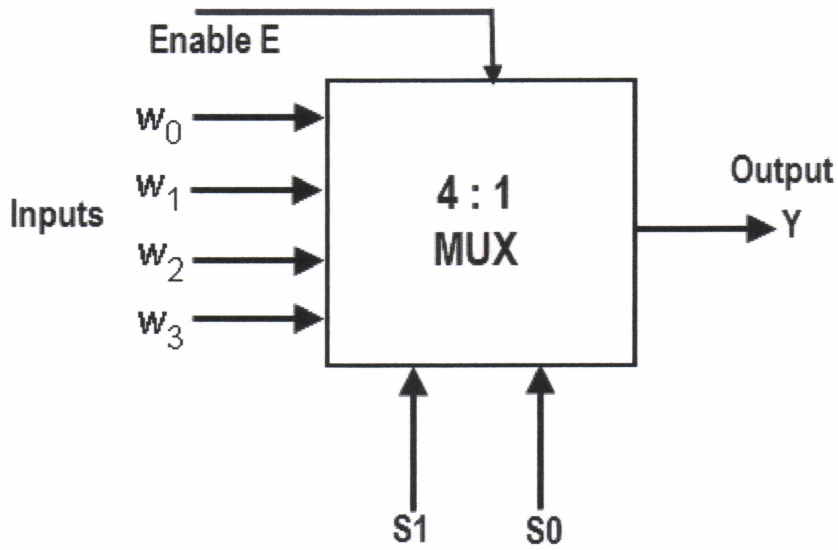
APPENDIX A

PIN ASSIGNMENT AND INTERNAL CIRCUITRY

4-to-1 Multiplexer



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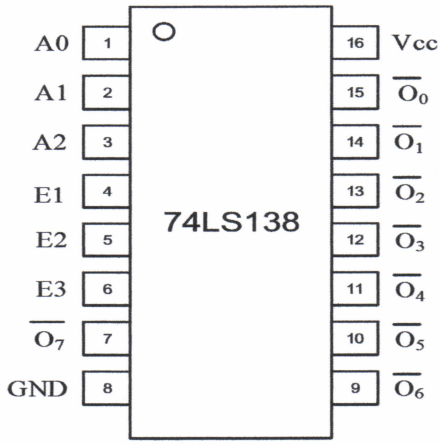
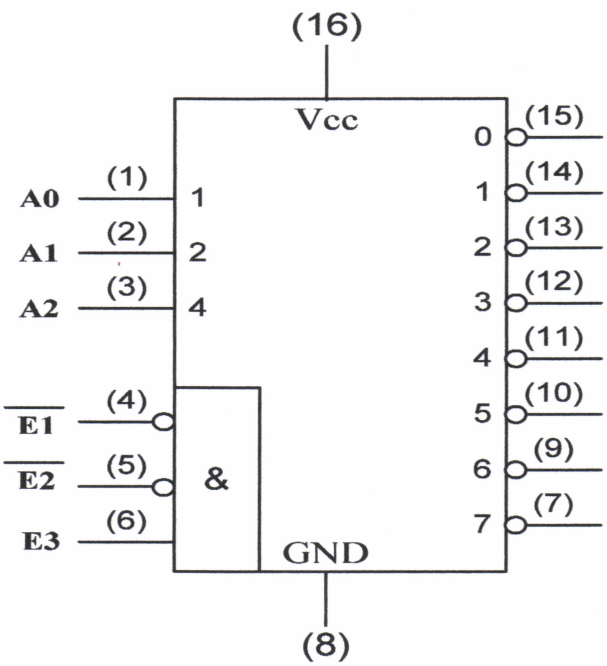
APPENDIX B

PIN ASSIGNMENT AND INTERNAL CIRCUITRY

74LS138 (3-to-8 Decoder)





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APPENDIX C