Universiti Tun Hussein Onn Malaysia

# UNIVERSITI TUN HUSSEIN ONN MALAYSIA

## FINAL EXAMINATION
## SEMESTER I
## SESSION 2017/2018

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|---|---|---|
| COURSE NAME | : | IC PACKAGING |
| COURSE CODE | : | BED 41103 |
| PROGRAMME | : | BEJ |
| EXAMINATION DATE | : | DECEMBER 2017 / JANUARY 2018 |
| DURATION | : | 3 HOURS |
| INSTRUCTION | : | ANSWER **ALL** QUESTIONS |



THIS QUESTION PAPER CONSISTS OF **THREE (3)** PAGES

**Q1** (a) Electronic products began shifting from vacuum tubes to the transistors in 1950s and into the integrated circuits (IC) in the 1960s. Continued advances in reducing the size of transistors allowed the progressive integration of tens, hundreds and thousands on a single IC.

(i) State the definition of IC.

(4 marks)

(ii) Give **TWO (2)** types of IC.

(4 marks)

(iii) Analyse **ALL** integration level of IC technologies.

(5 marks)

(b) Packaging is needed in all IC, which are classified into Through-Hole Technology (THT) and Surface Mount Technology (SMT). Both packages have their own unique packaging process flow.

(i) Compare the mounting difference between THT and SMT.

(6 marks)

(ii) Sketch and explain the flow of IC packaging process.

(6 marks)

**Q2** (a) Microelectronic packaging is designed to establish interconnections with electrical components such as transistors, diodes, capacitor and resistors to form circuits. It is also needed to ensure the chips and interconnections are packaged in an efficient and reliable manner.

(i) Describe **ALL** packaging levels in microelectronic packaging.

(3 marks)

(ii) Based on **Q2(a)(i)**, investigate the package item, function and electrochemical process at every packaging level.

(10 marks)

(b) The purpose of chip-package interconnection assembly is to enable an IC to be electrically connected to the package. These interconnection technologies include wire bond and tape automated bonding (TAB). With the aid of a diagram explain in detail of the process below:

(i) Wire Bond.



(4 marks)

(ii) Tape automated bond (TAB).

(4 marks)

(c) Comment on why wire bonding is still preferred as the main interconnection method compared to the flip chip and TAB.

(4 marks)

**Q3** (a) Failure mechanisms in an electronic product are major problem in production line. They are caused by thermo-mechanical, electrical, chemical and environmental mechanisms. Analyse **FIVE (5)** thermomechnical fundamentals.

(10 marks)

(b) The symptoms of failure in electronic devices are always observed at the system level. Understanding the mechanism that cause components failure are the key to make reliable microelectronic package.

(i) State **THREE (3)** failure mechanisms.

(6 marks)

(ii) Explain in detail the failure mechanisms in **Q3(b)(i)**.

(9 marks)

**Q4** (a) Encapsulation and sealing are two major protecting functions of IC packaging. They are used to protect IC devices from adverse environmental and mechanicals effect.

(i) Define encapsulation and sealing process.

(4 marks)

(ii) Compare encapsulation and sealing process.

(9 marks)

(b) Encapsulation provides both chemical and mechanical protection of IC, such that a reasonable life expectancy can be achieved under filed conditions in automotive, telecommunications, computer, consumer, medical and other industries. Encapsulation also can be considered as the middle process in IC packaging.

(i) Discuss the effect of encapsulation on the performance of electronic packaging.

(8 marks)

(ii) Differentiate between hermetic and non-hermetic material.

(4 marks)

**- END OF QUESTIONS -**