Universiti Tun Hussein Onn Malaysia

UNIVERSITI TUN HUSSEIN ONN MALAYSIA

FINAL EXAMINATION
SEMESTER I
SESSION 2017/2018

COURSE NAME	: DIGITAL DESIGN
COURSE CODE	: BEC 30503
PROGRAMME	: BEJ
EXAMINATION DATE	: DECEMBER 2017/JANUARY 2018
DURATION	: 3 HOURS
INSTRUCTION	: ANSWER ALL QUESTIONS

THIS QUESTION PAPER CONSISTS OF **SIX (6)** PAGES.

Q1 (a) Describe the different between Dataflow, Structural and Behavioral in Verilog Modelling Style.

(3 marks)

(b) Illustrate the circuit executed by the Verilog code as given in **Figure Q1 (b)**

(5 marks)

(c) Construct the Verilog code for the given circuit in **Figure Q2 (c)** by using hierarchical method. Use module in **Figure Q1(b)** as the lower-level module.

(12 marks)

Q2 (a) Convert the decimal numbers -87 into signed 8-bit numbers in the following representations:

(i) Sign and magnitude
(ii) 1's complement
(iii) 2's complement

(4 marks)

(b) **Figure Q2(b)** illustrates the FBD of a four-bit adder-subtractor for unsigned binary numbers using full adder modules. Write the Verilog gate-level hierarchical description for the four-bit adder-subtractor. Verilog code of full adder module is given in **Listing Q2(b)**. The mode input M controls the operation. When M = 0, the circuit is an adder, and when M = 1, the circuit becomes a subtractor.

(10 marks)

(c) Perform the following operations involving eight-bit 2's complement numbers and indicate whether arithmetic overflow occurs. Check your answers by converting to decimal sign-and-magnitude representation.

(i) 00110110 + 01000101
(ii) 01110101 − 11010110

(6 marks)

Q3 Controller is the sequential circuit that implement Finite State Machine (FSM). The design process of a controller begins with capturing the FSM's behavior and then converting the captured behavior into a circuit.

(a) Briefly discuss all substeps required to design a controller.

(5 marks)

(b) Consider the FSM of **Figure Q3(b)** that has an input a and an output y. Design a controller to implement the **Figure Q3(b)** using a state register and logic gates. Clearly show all the design steps.

(15 marks)

Q4 Suppose you are required to design a digital system that implements the function $f = x + 2y$ by using a datapath functional block diagram (FBD) given in **Figure Q4**. The circuit will only perform the operation when the *start* signal is asserted. The ALU operations are controlled by the Op signal as follows: Op = 0, F = A; Op = 1, F = A + B.

(a) Explain how to implement the "2*y*" computation by using the given ALU.

(2 marks)

(b) Write a Verilog code to model the given datapath unit (DU).

(7 marks)

(c) Sketch an ASM chart to model the RTL design. Furthermore, derive the RTL-CS table for the control unit (CU). The control vector (CV) should be arranged as follows: Ld1, Ld2, sel1, sel2, Op, En.

(7 marks)

(d) Sketch the FBD of the DU-CU integration for the complete design.

(4 marks)

Q5 Given equations below:

$$x = e \times (a + b + c) \qquad (1)$$

By applying coarse-level restructuring on the equation (1) to allow for minimal hardware implementation.

(a) Derive the data flow graph (DFG) and the schedule applying the constrained resource allocation of one multiplier and one adder. Also, apply "as late as possible" (ALAP) register allocation. The number of execution cycles should be as minimum as possible.

(8 marks)

(b) Derive the corresponding datapath unit (DU) based on the DFG in **Q5(a).**

(8 marks)

(c) It is given the propagation delays of the components are: adder = 20ns, multiplier = 100ns and register = 10ns. Perform performance analysis of your design by determining the maximum operating frequency and total execution time.

(4 marks)

-END OF QUESTIONS -

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```
module FA (Cin, x, y, s, Cout);

  input Cin, x, y;
  output s, Cout;

  assign s= x ^ y ^ Cin;
  assign Cout = (x & y) | (x & Cin) | ( y & Cin);

endmodule
```

Figure Q1 (b)

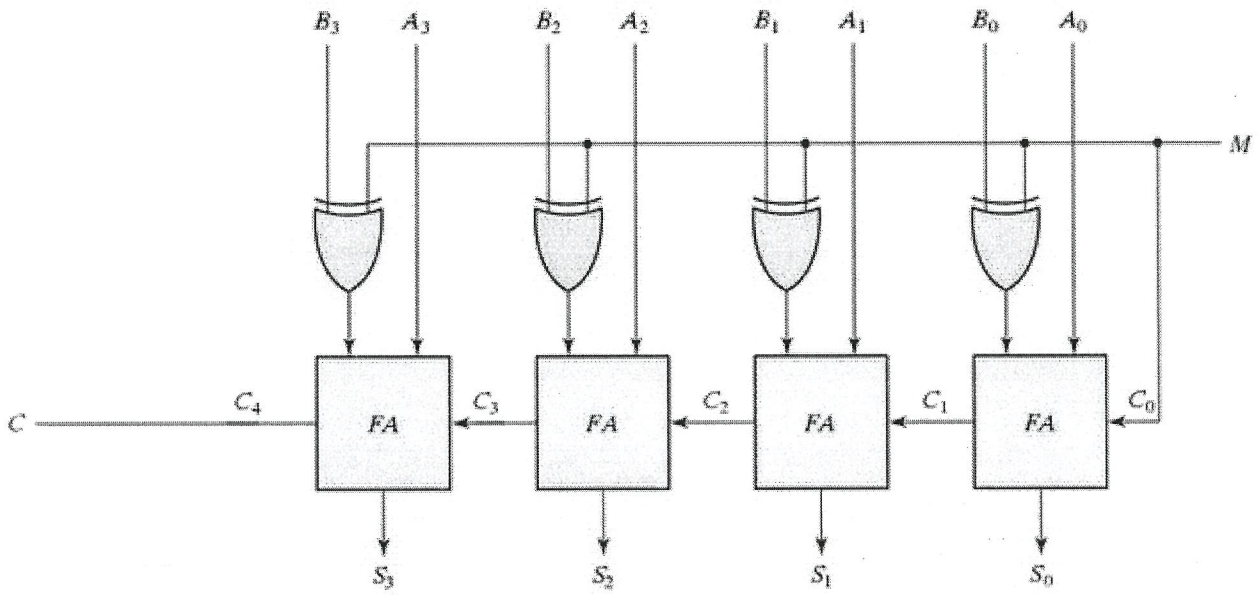

Figure Q2(b): Four-bit adder-subtractor

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```
module fulladd (ci, a, b, s, co);
   input ci, a, b;
   output s, co;

   assign s = a^b^ci;
   assign co = (a&b)|(a&ci)|(b&ci);
endmodule
```

Listing Q2(b)

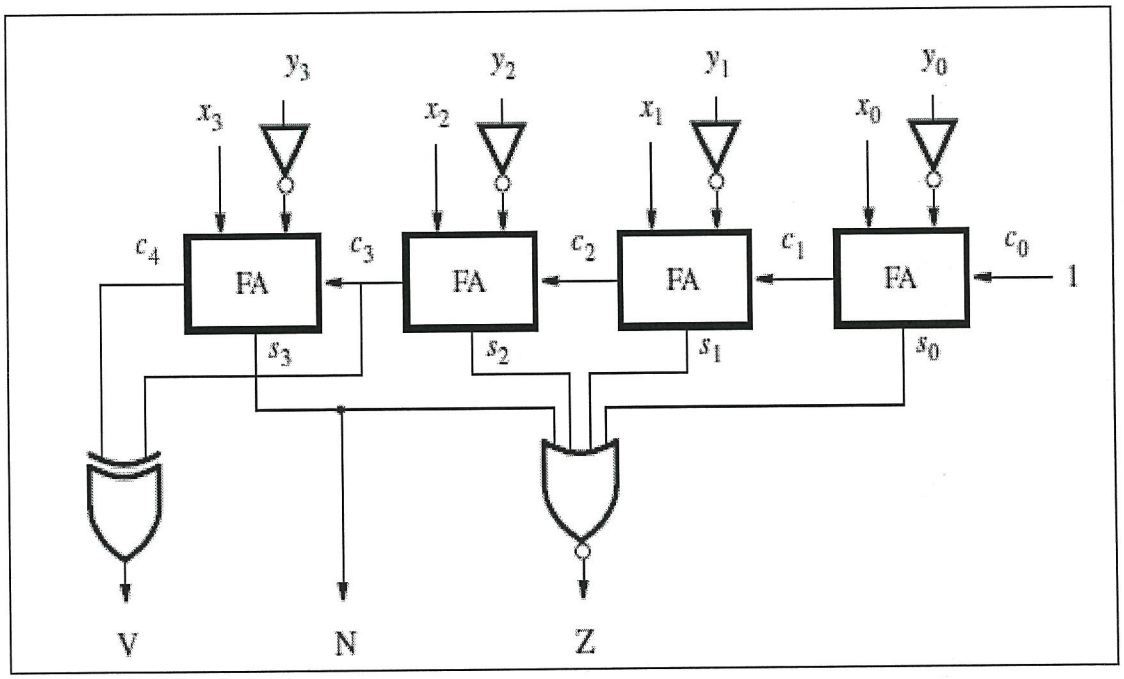

Figure Q2(c)

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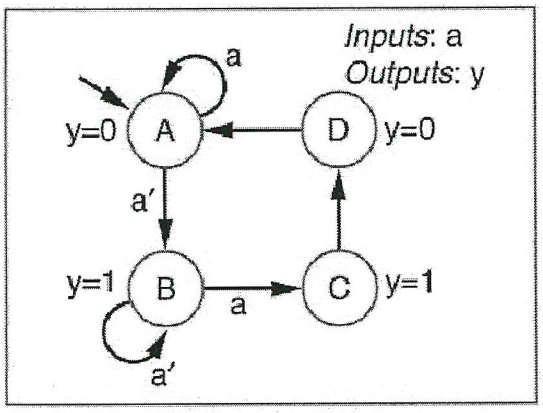

Figure Q3(b)

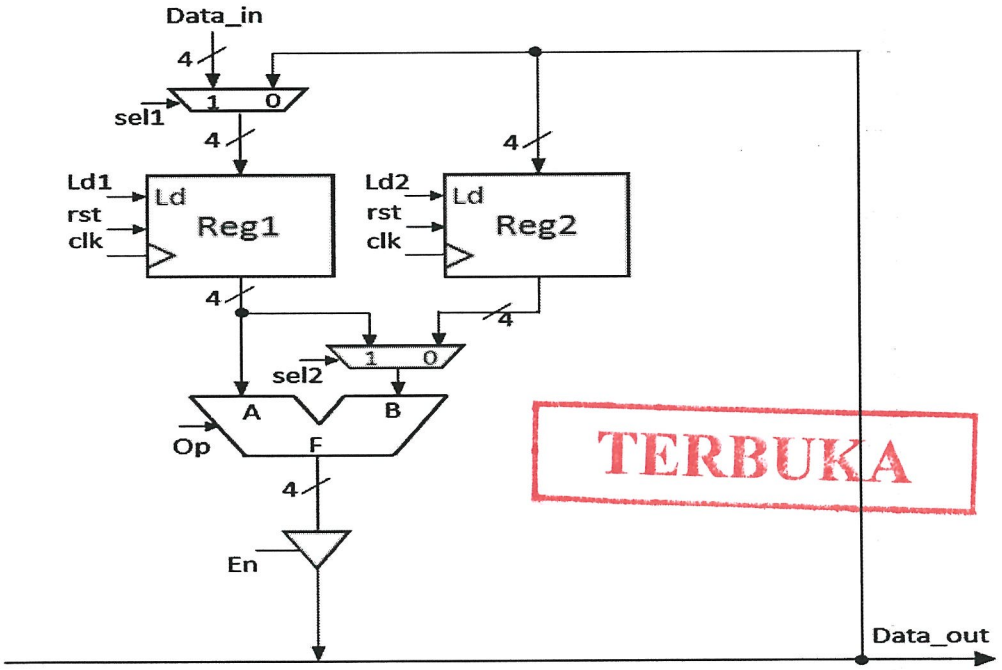

Figure Q4