Universiti Tun Hussein Onn Malaysia

# UNIVERSITI TUN HUSSEIN ONN MALAYSIA

## FINAL EXAMINATION
## SEMESTER I
## SESSION 2017/2018

| | | |
|---|---|---|
| COURSE NAME | : | DIGITAL ELECTRONICS |
| COURSE CODE | : | BEL 20303 |
| PROGRAMME | : | BEV/ BEJ |
| EXAMINATION DATE | : | DECEMBER 2017/ JANUARY 2018 |
| DURATION | : | 3 HOURS |
| INSTRUCTION | : | 1. ANSWER **ALL** QUESTIONS IN THIS BOOKLET.<br>2. **NO CALCULATOR** IS ALLOWED. |

THIS QUESTION PAPER CONSISTS OF **FOURTEEN (14)** PAGES

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**Q1** (a) Convert BCD code 0110 0010 1001 to hexadecimal. Show all the steps.

(3 marks)

(b) Convert the octal number 547 to Gray code. Show all the steps.

(3 marks)

(c) Convert the binary number 0.0110 to decimal. Show all the steps.

(3 marks)

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(d) Using 7 bits to represent each number, write the representations of 23 and -23 in signed magnitude, 1's complement and 2's complement integers.

(6 marks)

(e) **Figure Q1(e)** shows a combinational circuit with 3 inputs, A, B and C and 1 output, Z. Input A is the MSB whereas input C is the LSB. Analyze **Figure Q1(e)** and obtain the simplest Boolean expression for Z using Boolean theorem.

(4 marks)

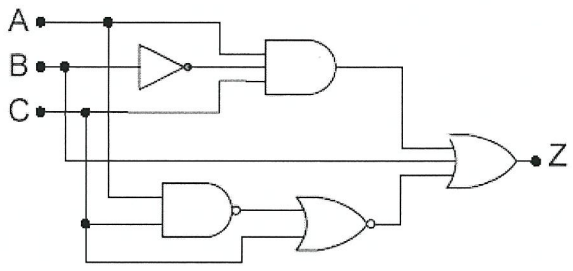


**Figure Q1(e)**

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(f) By using Boolean theorem, analyze either the two circuits given in **Figure Q1(f)** implement the same function or not (do not use a truth table or Karnaugh map).

(6 marks)

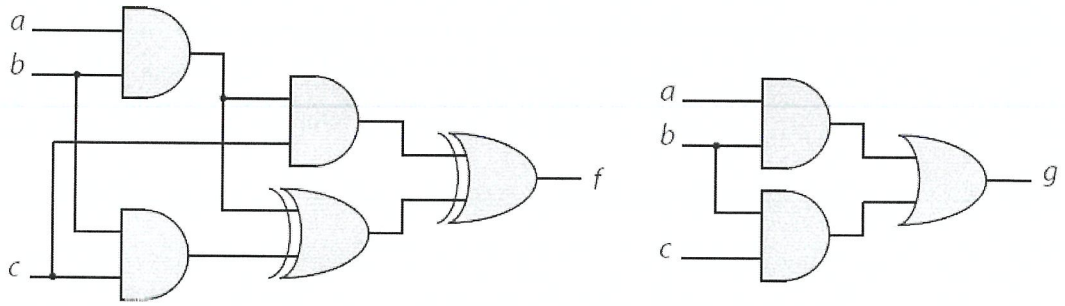


**Figure Q1(f)**

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**Q2** (a) Examine the minimum number of gate logic by simplifying the combinational logic circuit in **Figure 2(a)** to a minimum form.

(5 marks)

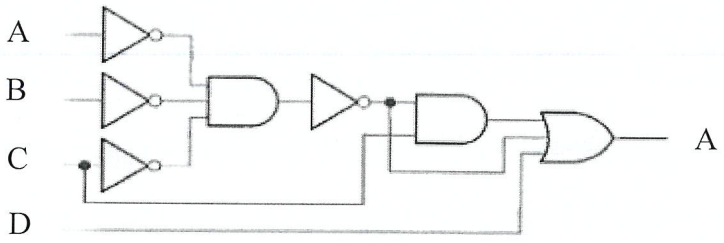


**Figure 2(a)**

(b) Given the Boolean expression, $X = \overline{\bar{A}.(\bar{B}.C)}.D$

(i) Implement the expression $X$ using NOT, AND and NAND gates.

(3 marks)

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(ii) Implement the expression using only NOR gates.

(6 marks)

(c) A jet aircraft employs a system for monitoring the rpm, pressure and temperature values of its engines using sensors that operate as follows:

Temperature sensor, $T = 0$ only when temperature < 200 F
Pressure sensor, $P = 0$ only when pressure < 220 psi
RPM sensor, $R = 0$ only when speed < 4800 rpm

Sensors output $T$, $P$ and $R$ will be 1 if they exceed their maximum limits or else 0. Pilot will be given a warning when the temperature of the engine is more than 200F and either engine pressure is more than 220 psi or the engine speed is less than 4800 rpm. Assume that a HIGH at output W activates the warning light.

(i) Obtain the truth table for this circuit.

(5 marks)

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(ii) By using Karnaugh map, write the simplest Boolean expression for W.
(4 marks)

(iii) Draw the schematic diagram for W based on its Boolean expression in **Q2(b).**
(2 marks)

**Q3** (a) Briefly explain the demultiplexer (DEMUX) by the aid of diagram.
(4 marks)

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(b) Design a half adder circuit using only 2-input NAND gates.

(5 marks)

(c) A valve control circuit has three inputs (x,y,z) and two outputs (A, B). The circuit is implemented using two 4-to-1 multiplexer IC as shown in **Figure Q3(a).** Based on the circuit:

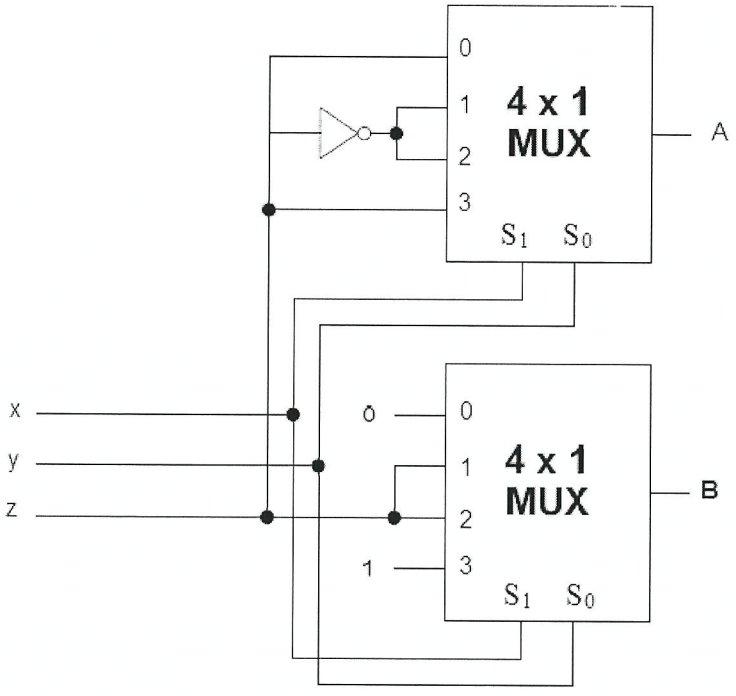


**Figure Q3(a)**

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(i) Derive the truth table

(6 marks)

(ii) Determine the outputs function A and B in Sum of Product (SOP).

(4 marks)

(d) Implement the following Boolean function using a 3 × 8 decoder plus any logic gates needed. The pin assignment and schematic diagram of IC74LS138 (3-to-8 decoder) is given in **Appendix A**.

$$F = a\bar{b} + \bar{b}c + \bar{a}b\bar{c}$$

(6 marks)

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**Q4** (a) An asynchronous counter circuit is given in **Figure Q4(a)(i)**. Analyze the sequence of the counter and complete the timing diagram provided in **Figure Q4(a)(ii)**.
(6 marks)

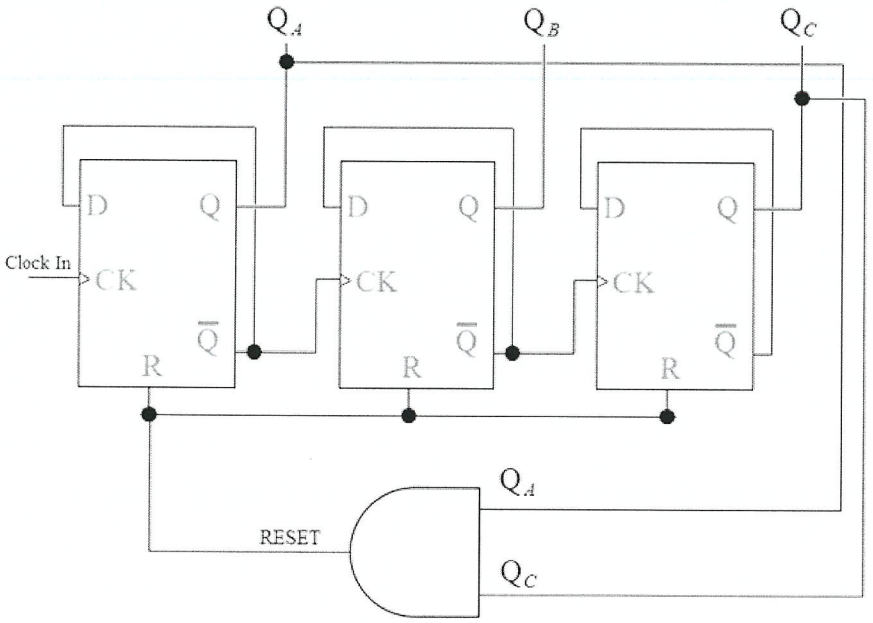


**Figure Q4(a)(i)**

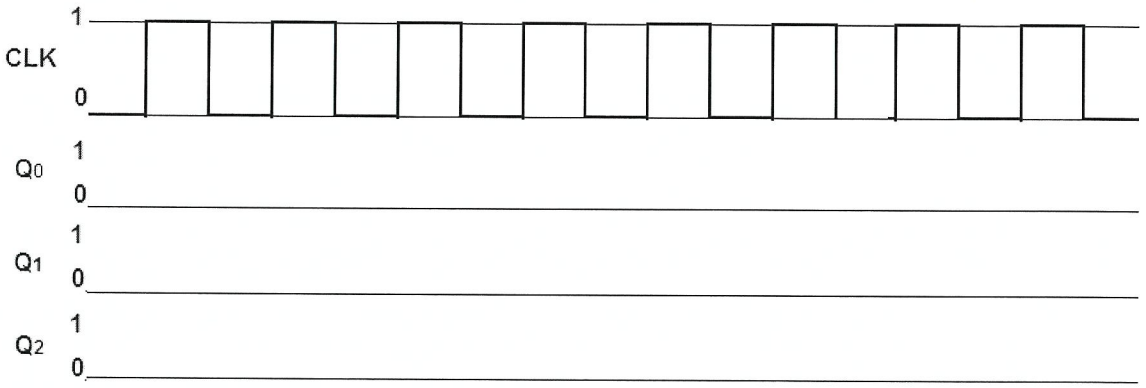


**Figure Q4(a)(ii)**

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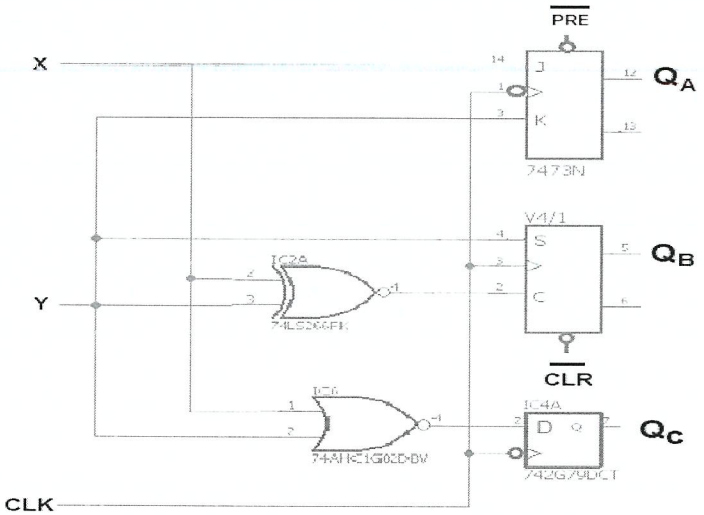
(b) Given the circuit diagram in **Figure Q5(a)**, determine the timing diagram for $Q_A$, $Q_B$, and $Q_C$ in **Figure Q5(b)**. Assume that $Q_A$, $Q_B$, and $Q_C$ are in high state initially.

(6 marks)

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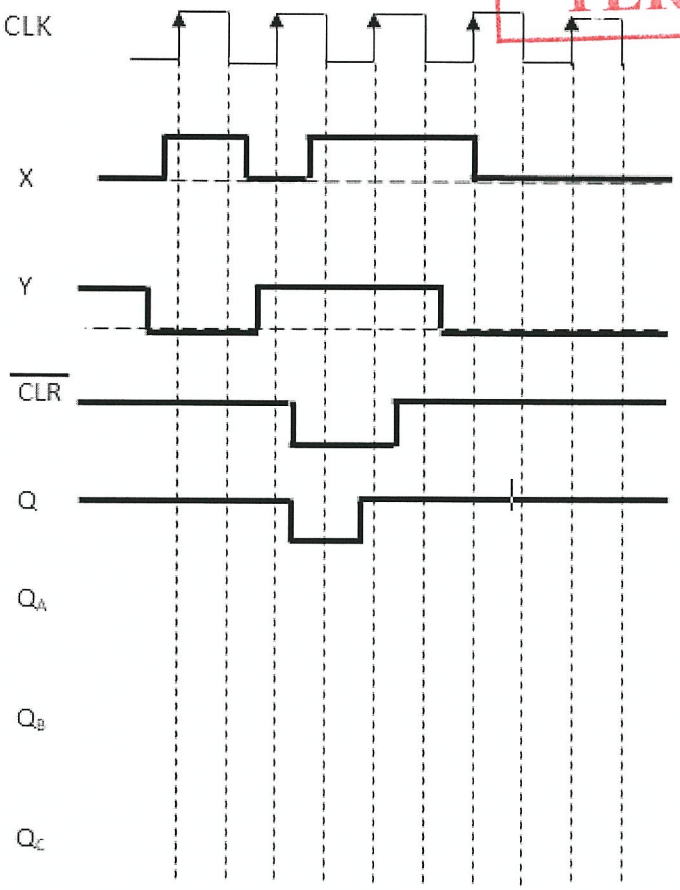


**Figure Q4(b)**

(c) Design a 3-bit binary synchronous down-counter using J-K flip-flops. In your design, include the following:

(i) Draw the state diagram

(1 marks)

(ii) Prepare an excitation table for this state machine Assume the J-K flip-flops are rising-edge-triggered

(4 marks)

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(iii) Analyze the simplest Boolean expression using Karnaugh map

(6 marks)

(iv) Implement the circuit diagram

(2 marks)

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**- END OF QUESTIONS -**

**FINAL EXAMINATION**

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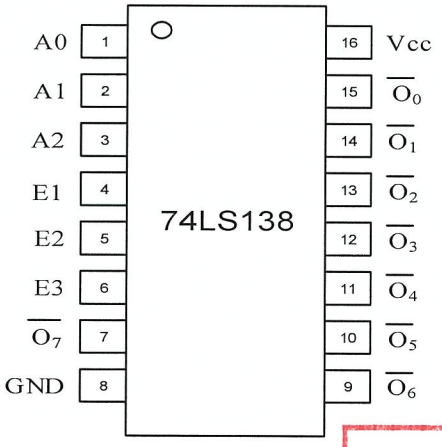
# APPENDIX A

## PIN ASSIGNMENT AND INTERNAL CIRCUITRY

**74LS138 (3-to-8 Decoder)**

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