UTHM
Universiti Tun Hussein Onn Malaysia

# UNIVERSITI TUN HUSSEIN ONN MALAYSIA

## FINAL EXAMINATION
## SEMESTER II
## SESSION 2018/2019

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|---|---|---|
| COURSE NAME | : | ANALOG ELECTRONICS |
| COURSE CODE | : | BEJ 10503 |
| PROGRAMME | : | BEJ |
| EXAMINATION DATE | : | JUNE / JULY 2019 |
| DURATION | : | 3 HOURS |
| INSTRUCTION | : | ANSWER **ALL** QUESTIONS |

THIS QUESTION PAPER CONSISTS OF **SEVEN** (7) PAGES

**Q1** (a) Describe in your own words the depletion region during forward bias condition on a P-N junction.

(2 marks)

(b) Zener diode can be used as a voltage regulator for providing stable constant reference voltages.

(i) Explain how a Zener diode can be used to regulate a DC voltage.

(2 marks)

(ii) Determine the range of input voltage, $V_i$ that will maintain the Zener diode shown in **Figure Q1(b)(ii)** is in the "ON" state. Show your calculations to support your answers.

(6 marks)

**Q2** (a) Define **THREE (3)** basic operating modes of a bipolar junction transistor (BJT) and the bias condition of its Base-Emitter (BE) and Collector-Emitter (CE) junction at each mode.

(9 marks)

(b) **Figure Q2(b)** shows a BJT with voltage divider configuration connected to a 200 µF capacitor at the input and output terminals. The device has the output characteristics $I_{CQ}$ and $V_{CEQ}$ of 2 mA and 10 V, respectively. Analyze the circuit and calculate,

(i) the base voltage, $V_B$.

(3 marks)

(ii) the value of $R_1$.

(2 marks)

(iii) the value of $R_C$.

(2 marks)

(c) An additional capacitor of 100 µF is connected in parallel with the resistor $R_E$ for **Figure Q2(b)** and $\beta$ of the device is 100. $Z_i$ and $Z_o$ represent both input and output impedances of the circuit respectively.

(i) Round the the resistance values of $R_1$ and $R_C$ in part **Q2(b)** to integer number.

(2 marks)

(ii) Given the value of $r_o = \infty$, draw the AC equivalent circuit and calculate $r_e$.

(4 marks)

(iii) By using small signal analysis, evaluate the input impedance, $Z_i$, output impedance, $Z_o$, voltage gain and current gain if load resistance, $R_L$, is given as 5 kΩ.

(8 marks)

**Q3** (a) The two main types of field-effect transistors (FETs) are the junction field-effect transistor (JFET) and the metal oxide semiconductor field-effect transistor (MOSFET).

(i) With the aid of diagram, briefly explain the operating conditions for a JFET in the ohmic and active region.

(6 marks)

(ii) List **THREE (3)** comparisons between JFET and MOSFET.

(3 marks)

(b) Design a self-bias amplifier circuit using n-channel JFET with $I_{DQ}$ = 4.5 mA. Given $I_{DSS}$ = 10 mA, $V_P$ = -8 V, and $V_{DD}$ = 12 V. Assume $R_D = 3R_S$ and $R_G$ = 10 MΩ.

(10 marks)

(c) Based on the amplifier circuit with common-source voltage divider configuration shown in **Figure Q3(c)**.

(i) sketch the AC equivalent circuit.

(3 marks)

(ii) determine the input impedance, $Z_i$, output impedance, $Z_o$ and voltage gain, $A_v$ if the resulting of $V_{GSQ}$ and $I_{DQ}$ are 0.35 V and 7.6 mA, respectively.

(8 marks)

**Q4** (a) **Figure Q4(a)** is an amplifier circuit that only amplifies the signals of specified frequencies. Assume that the BJT transistor has an infinite value of AC collector resistance, $r_o$ (or $r_c$):

(i) compute $r_e$ .

(6 marks)

(ii) draw its AC equivalent circuit for low frequency response.

(3 marks)

(iii) determine the low cut-off frequencies $f_{LC}$, $f_{LS}$ and $f_{LE}$.

(10 marks)

(iv) state the dominant low cut-off frequency, $f_L$ and sketch the frequency response.

(3 marks)

(b) **Figure Q4(b)** shows the class-B power amplifier circuit. Given that Rb1 = Rb2 = 3.9 kΩ, supply voltage, ±Vcc = ±20 V, Rload =10 Ω, Rin = 47 Ω and Cin = 1 μF. Based on this figure;

(i) compute the circuit efficiency if the peak output voltage, $V_{out\ (peak)}$ across the Rload is 10V.

(3 marks)

(ii) design a class AB amplifier by modifying circuit in **Figure Q4(b).** Draw the circuit and determine the maximum efficiency of the modified circuit.

(5 marks)

- END OF QUESTIONS -

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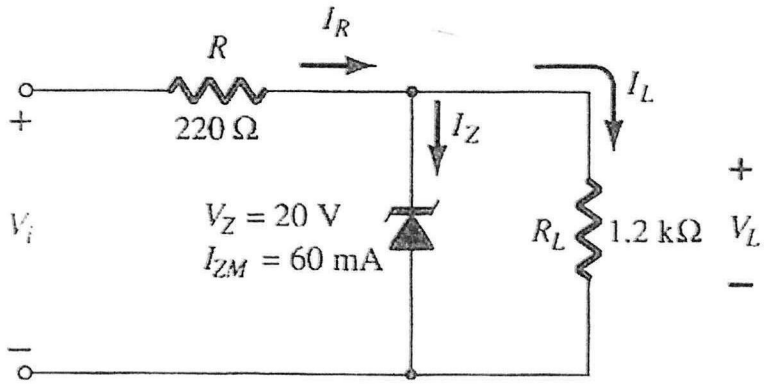


**Figure Q1(b)(ii)**

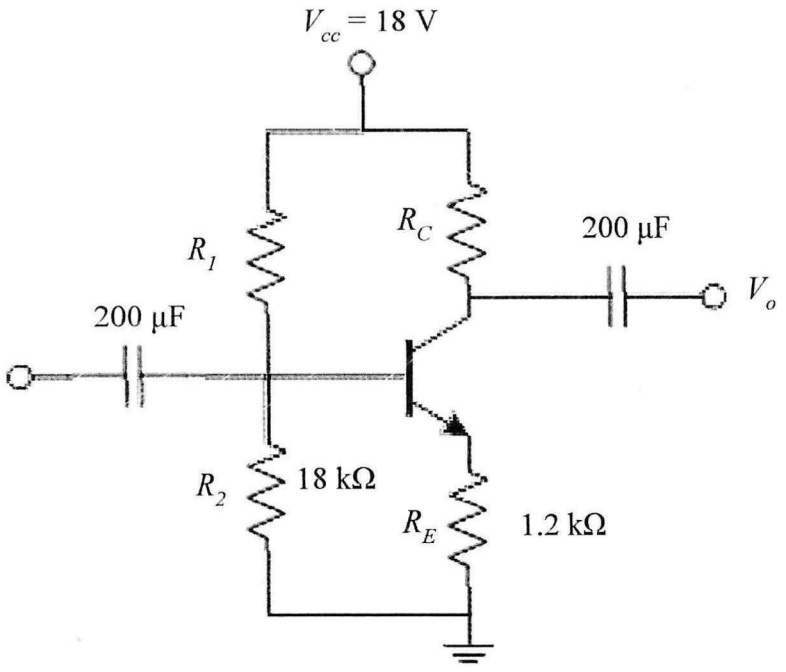


**Figure Q2(b)**

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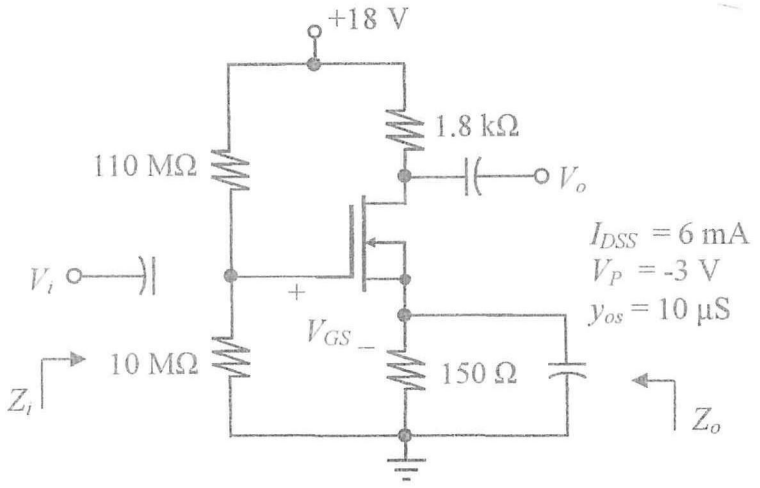


**Figure Q3(c)**

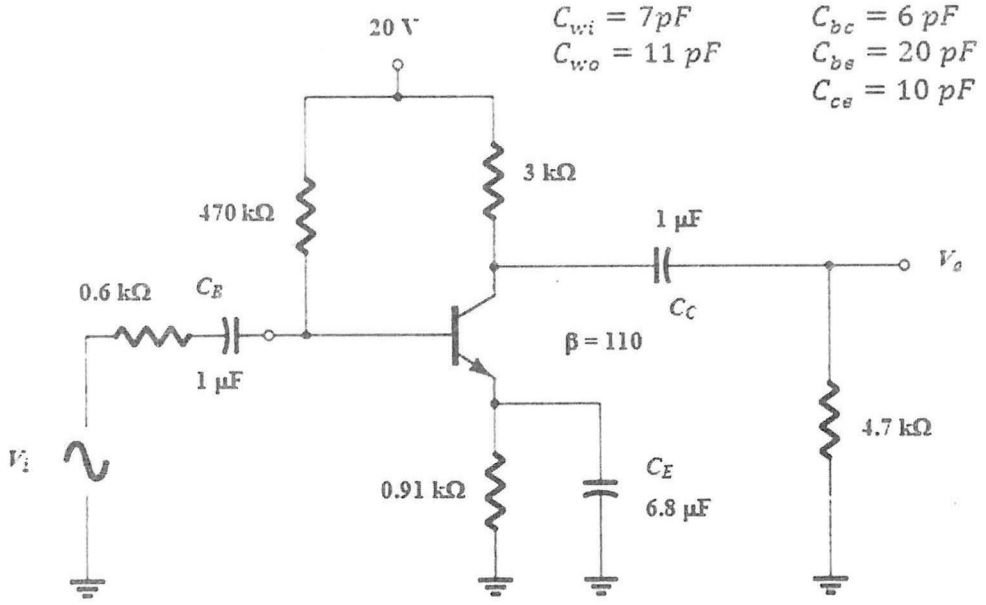


**Figure Q4(a)**

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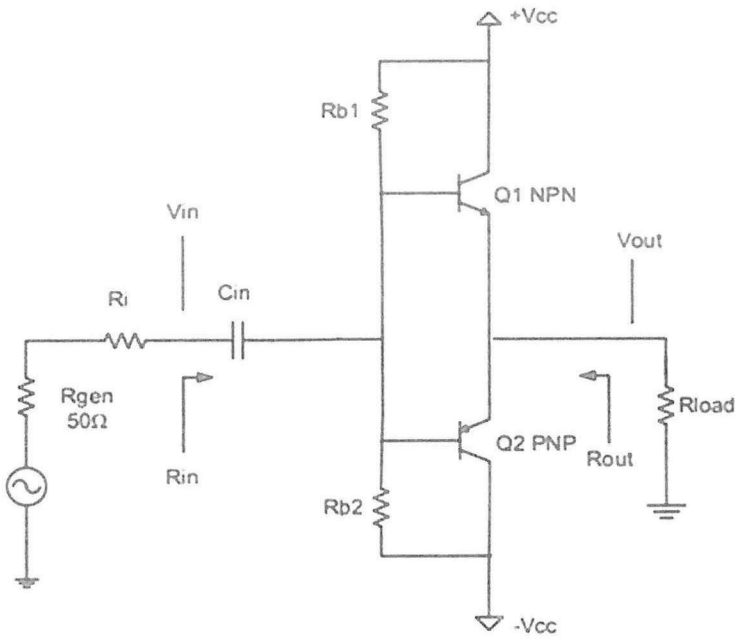


Figure Q4(b)