



UNIVERSITI TUN HUSSEIN ONN MALAYSIA

**FINAL EXAMINATION
SEMESTER II
SESSION 2017/2018**

COURSE NAME : MICROCONTROLLER
APPLICATION

COURSE CODE : BNR 35503

PROGRAMME CODE : BND / BNE

EXAMINATION DATE : JUNE / JULY 2018

DURATION : 2 HOURS 30 MINUTES

INSTRUCTION : ANSWER ALL QUESTIONS

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THIS QUESTION PAPER CONSISTS OF **FIFTEEN (15)** PAGES

- Q1**
- (a) List **FOUR(4)** interrupt sources in PIC18F4550. (4 marks)
 - (b) Given the clock input for the PIC18F4550 is 4 MHz. Calculate the value to be loaded into TMR0 registers <TMR0H:TMR0L> based on 16 bit timer configuration and suggest the prescale value to be used for the TMR0 overflow every 1024 μ s. (8 marks)
 - (c) Suggest and explain the value of INTCON register if the specifications are as in **Question 1(b)**. (4 marks)
 - (d) If the PIC 18F4550 is connected to a LED as shown in **Figure Q1(d)**. Write a simple program to blink the LED every 1024 μ s using specifications as in **Question 1(b)**. (7 marks)
 - (e) Explain the advantage of using TMR0 overflow interrupt as compared to the polling on T0IF flag method. (2 marks)
- Q2** **Figure Q2** shows a simple application using PIC 18F4550 to read two analogs input via RA0 and RA1 pins. There are two LEDs connected to RB0 and RB1 respectively. RB2 is connected to another output called output 1. The PIC is clocked at 8MHz.
- (a) Determine and explain the initialization value of ADCON0 to implement the circuit in **Figure Q2**. Suggest the best value for ADCON1 and ADCON2. (5 marks)
 - (b) Write a sequence of C code to initialize the ADC with left-justified output. (5 marks)
 - (c) Prepare a simple C code that read analog input from RA0 and transfer ADRESH output into LATC. Then read from RA1 and transfer ADRESH into LATD. (Hint: Make sure ADC configuration registers are set properly) (6 marks)
 - (d) Referring to **Figure Q2**, write a simple C program to light the LED1 when the analog value of RA0 is greater than RA1 and light the LED2 when the analog value of RA1 is greater than RA0. (9 marks)

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- Q3** (a) List **THREE (3)** factors that may affect the speed of a motor. (3 marks)
- (b) Determine a suitable value for PR2 and the prescaler needed to get 4.88 kHz PWM frequency. Assume XTAL = 20 MHz. (4 marks)
- (c) Construct a code for creating square wave of 30% duty cycle on the PORTB bit 0. Timer2 is used to generate the time delay and the PWM frequency is 4.88 kHz. (14 marks)
- (d) Demonstrate the representation of 30% duty cycle with 4.88 kHz PWM frequency in CCP1L and CCP1CON register. (4 marks)
- Q4** (a) The PIC18 transfers and receives data serially at many different baud rates. The baud rate is reprogrammable with the 8-bit register called SPBRG.
- (i) For XTAL = 10 MHz, calculate the SPBRG value (in both decimal and hex) for baud rates 9600. (3 marks)
- (ii) Investigate the SPBRG value (in both decimal and hex) for **Question 4(a)(i)**. Given that the value of BRGH bit of TXSTA register is HIGH. (3 marks)
- (iii) Calculate the baud rate error for **Question 4(a)(i)**. (3 marks)
- (b) Create a C program based on the following statement:
“PIC18 gets data from PORTD and send it to TXREG continuously while incoming data from the serial port is sent to PORTB. Assume that XTAL = 10 MHz and the baud rate is 9600” (16 marks)

- END OF QUESTIONS -

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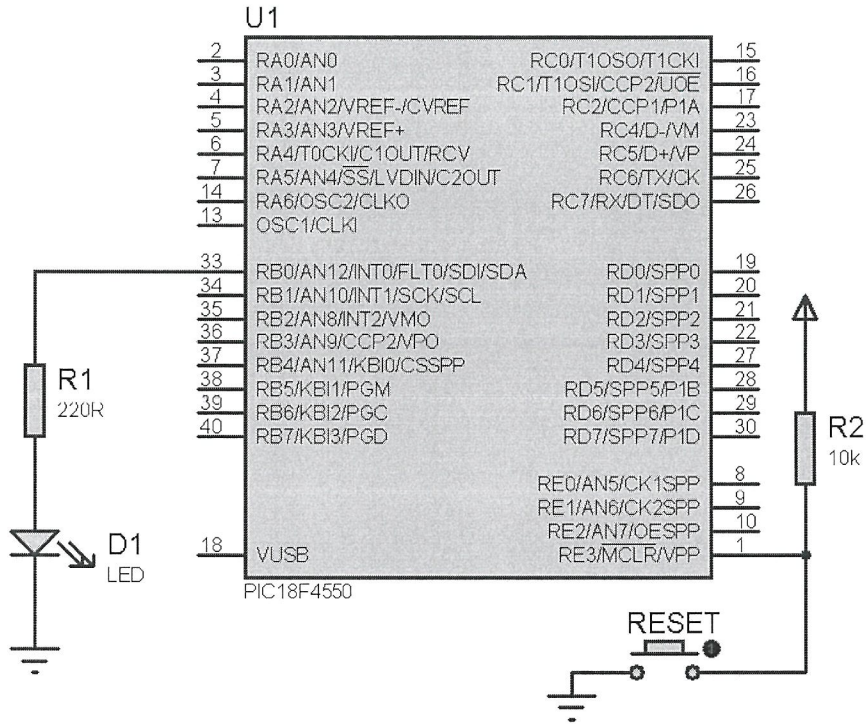


Figure Q1(d)

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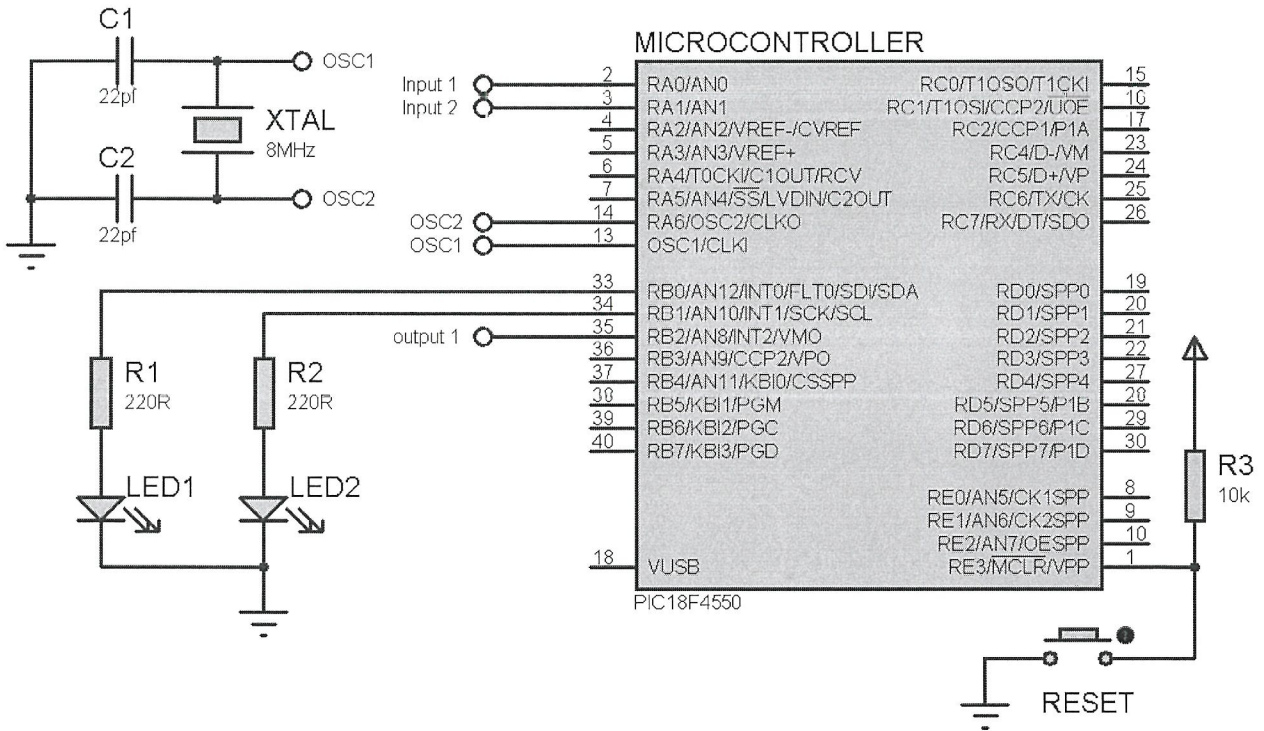


Figure Q2

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APPENDIX I : SPECIAL FUNCTION REGISTER (SFR)

Address	Name	Address	Name	Address	Name	Address	Name	Address	Name
FFFh	TOSU	FDfh	INDF2 ⁽¹⁾	FBFh	CCPR1H	F9Fh	IPR1	F7Fh	UEP15
FFEh	TOSH	FDEh	POSTINC2 ⁽¹⁾	FBEh	CCPR1L	F9Eh	PIR1	F7Eh	UEP14
FFDh	TOSL	FDDh	POSTDEC2 ⁽¹⁾	FBDh	CCP1CON	F9Dh	PIE1	F7Dh	UEP13
FFCh	STKPTR	FDCh	PREINC2 ⁽¹⁾	FBCh	CCPR2H	F9Ch	— ⁽²⁾	F7Ch	UEP12
FFBh	PCLATU	FDBh	PLUSW2 ⁽¹⁾	FBBh	CCPR2L	F9Bh	OSCTUNE	F7Bh	UEP11
FFAh	PCLATH	FDAh	FSR2H	FBAh	CCP2CON	F9Ah	— ⁽²⁾	F7Ah	UEP10
FF9h	PCL	FD9h	FSR2L	FB9h	— ⁽²⁾	F99h	— ⁽²⁾	F79h	UEP9
FF8h	TBLPTRU	FD8h	STATUS	FB8h	BAUDCON	F98h	— ⁽²⁾	F78h	UEP8
FF7h	IBLPIRH	FD7h	TMR0H	FB7h	ECCP1DEL	F97h	— ⁽²⁾	F77h	UEP7
FF6h	TBLPTRL	FD6h	TMR0L	FB6h	ECCP1AS	F96h	TRISE ⁽³⁾	F76h	UEP6
FF5h	TABLAT	FD5h	T0CON	FB5h	CVRCON	F95h	TRISD ⁽³⁾	F75h	UEP5
FF4h	PRODH	FD4h	— ⁽²⁾	FB4h	CMCON	F94h	TRISC	F74h	UEP4
FF3h	PRODL	FD3h	OSCCON	FB3h	TMR3H	F93h	TRISB	F73h	UEP3
FF2h	INTCON	FD2h	HLVDCON	FB2h	TMR3L	F92h	TRISA	F72h	UEP2
FF1h	INTCON2	FD1h	WDTCON	FB1h	T3CON	F91h	— ⁽²⁾	F71h	UEP1
FF0h	INTCON3	FD0h	RCON	FB0h	SPBRGH	F90h	— ⁽²⁾	F70h	UEP0
FEFh	INDF0 ⁽¹⁾	FCfh	TMR1H	FAfh	SPBRG	F8Fh	— ⁽²⁾	F6Fh	UCFG
FEeh	POSTINC0 ⁽¹⁾	FCEh	TMR1L	FAeh	RCREG	F8Eh	— ⁽²⁾	F6Eh	UADDR
FECh	POSTDEC0 ⁽¹⁾	FCDh	T1CON	FADh	TXREG	F8Dh	LATE ⁽³⁾	F6Dh	UCON
FECh	PREINC0 ⁽¹⁾	FCCh	TMR2	FACH	TXSTA	F8Ch	LATD ⁽³⁾	F6Ch	USTAT
FEbh	PLUSW0 ⁽¹⁾	FCBh	PR2	FABh	RCSTA	F8Bh	LATC	F6Bh	UEIE
FEAh	FSR0H	FCAh	T2CON	FAAh	— ⁽²⁾	F8Ah	LATB	F6Ah	UEIR
FE9h	FSR0L	FC9h	SSPBUF	FA9h	EEADR	F89h	LATA	F69h	UIE
FE8h	WREG	FC8h	SSPADD	FA8h	EEDATA	F88h	— ⁽²⁾	F68h	UIR
FE7h	INDF1 ⁽¹⁾	FC7h	SSPSTAT	FA7h	ECON2 ⁽¹⁾	F87h	— ⁽²⁾	F67h	UFRMH
FE6h	POSTINC1 ⁽¹⁾	FC6h	SSPCON1	FA6h	ECON1	F86h	— ⁽²⁾	F66h	UFRML
FE5h	POSTDEC1 ⁽¹⁾	FC5h	SSPCON2	FA5h	— ⁽²⁾	F85h	— ⁽²⁾	F65h	SPPCON ⁽³⁾
FE4h	PREINC1 ⁽¹⁾	FC4h	ADRESH	FA4h	— ⁽²⁾	F84h	PORTE	F64h	SPPEPS ⁽³⁾
FE3h	PLUSW1 ⁽¹⁾	FC3h	ADRESL	FA3h	— ⁽²⁾	F83h	PORTD ⁽³⁾	F63h	SPPCFG ⁽³⁾
FE2h	FSR1H	FC2h	ADCON0	FA2h	IPR2	F82h	PORTC	F62h	SPPDATA ⁽³⁾
FE1h	FSR1L	FC1h	ADCON1	FA1h	PIR2	F81h	PORTB	F61h	— ⁽²⁾
FE0h	BSR	FC0h	ADCON2	FA0h	PIE2	F80h	PORTA	F60h	— ⁽²⁾



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APPENDIX II : INTERRUPT CONTROL REGISTER (INTCON)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-x
GIE/GIEH	PEIE/GIEL	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF ⁽¹⁾
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

- bit 7 **GIE/GIEH:** Global Interrupt Enable bit
 When IPEN = 0:
 1 = Enables all unmasked interrupts
 0 = Disables all interrupts
 When IPEN = 1:
 1 = Enables all high-priority interrupts
 0 = Disables all interrupts
- bit 6 **PEIE/GIEL:** Peripheral Interrupt Enable bit
 When IPEN = 0:
 1 = Enables all unmasked peripheral interrupts
 0 = Disables all peripheral interrupts
 When IPEN = 1:
 1 = Enables all low-priority peripheral interrupts (if GIE/GIEH = 1)
 0 = Disables all low-priority peripheral interrupts
- bit 5 **TMR0IE:** TMR0 Overflow Interrupt Enable bit
 1 = Enables the TMR0 overflow interrupt
 0 = Disables the TMR0 overflow interrupt
- bit 4 **INT0IE:** INT0 External Interrupt Enable bit
 1 = Enables the INT0 external interrupt
 0 = Disables the INT0 external interrupt
- bit 3 **RBIE:** RB Port Change Interrupt Enable bit
 1 = Enables the RB port change interrupt
 0 = Disables the RB port change interrupt
- bit 2 **TMR0IF:** TMR0 Overflow Interrupt Flag bit
 1 = TMR0 register has overflowed (must be cleared in software)
 0 = TMR0 register did not overflow
- bit 1 **INT0IF:** INT0 External Interrupt Flag bit
 1 = The INT0 external interrupt occurred (must be cleared in software)
 0 = The INT0 external interrupt did not occur
- bit 0 **RBIF:** RB Port Change Interrupt Flag bit⁽¹⁾
 1 = At least one of the RB7:RB4 pins changed state (must be cleared in software)
 0 = None of the RB7:RB4 pins have changed state



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APPENDIX V : A/D CONTROL REGISTER 1 (ADCON1)

U-0	U-0	R/W-0	R/W-0	R/W-0 ⁽¹⁾	R/W ⁽¹⁾	R/W ⁽¹⁾	R/W ⁽¹⁾
—	—	VCFG1	VCFG0	PCFG3	PCFG2	PCFG1	PCFG0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-6 **Unimplemented:** Read as '0'

bit 5 **VCFG1:** Voltage Reference Configuration bit (VREF- source)
 1 = VREF- (AN2)
 0 = Vss

bit 4 **VCFG0:** Voltage Reference Configuration bit (VREF+ source)
 1 = VREF+ (AN3)
 0 = VDD

bit 3-0 **PCFG3:PCFG0:** A/D Port Configuration Control bits:

PCFG3: PCFG0	AN12	AN11	AN10	AN9	AN8	AN7 ⁽²⁾	AN6 ⁽²⁾	AN5 ⁽²⁾	AN4	AN3	AN2	AN1	AN0
0000 ⁽¹⁾	A	A	A	A	A	A	A	A	A	A	A	A	A
0001	A	A	A	A	A	A	A	A	A	A	A	A	A
0010	A	A	A	A	A	A	A	A	A	A	A	A	A
0011	D	A	A	A	A	A	A	A	A	A	A	A	A
0100	D	D	A	A	A	A	A	A	A	A	A	A	A
0101	D	D	D	A	A	A	A	A	A	A	A	A	A
0110	D	D	D	D	A	A	A	A	A	A	A	A	A
0111 ⁽¹⁾	D	D	D	D	D	A	A	A	A	A	A	A	A
1000	D	D	D	D	D	D	A	A	A	A	A	A	A
1001	D	D	D	D	D	D	D	A	A	A	A	A	A
1010	D	D	D	D	D	D	D	D	A	A	A	A	A
1011	D	D	D	D	D	D	D	D	D	A	A	A	A
1100	D	D	D	D	D	D	D	D	D	D	A	A	A
1101	D	D	D	D	D	D	D	D	D	D	D	A	A
1110	D	D	D	D	D	D	D	D	D	D	D	D	A
1111	D	D	D	D	D	D	D	D	D	D	D	D	D

A = Analog input

D = Digital I/O



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APPENDIX VII : ECCP CONTROL REGISTER (CCP1CON)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
P1M1	P1M0	DC1B1	DC1B0	CCP1M3	CCP1M2	CCP1M1	CCP1M0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

- bit 7-6 **P1M1:P1M0:** Enhanced PWM Output Configuration bits
If CCP1M3:CCP1M2 = 00, 01, 10:
 ::: = P1A assigned as Capture/Compare input/output; P1B, P1C, P1D assigned as port pins
If CCP1M3:CCP1M2 = 11:
 00 = Single output: P1A modulated; P1B, P1C, P1D assigned as port pins
 01 = Full-bridge output forward: P1D modulated; P1A active; P1B, P1C inactive
 10 = Half-bridge output: P1A, P1B modulated with dead-band control; P1C, P1D assigned as port pins
 11 = Full-bridge output reverse: P1B modulated; P1C active; P1A, P1D inactive
- bit 5-4 **DC1B1:DC1B0:** PWM Duty Cycle Bit 1 and Bit 0
Capture mode:
 Unused.
Compare mode:
 Unused.
PWM mode:
 These bits are the two LSBs of the 10-bit PWM duty cycle. The eight MSBs of the duty cycle are found in CCPR1L.
- bit 3-0 **CCP1M3:CCP1M0:** Enhanced CCP Mode Select bits
 0000 = Capture/Compare/PWM off (resets ECCP module)
 0001 = Reserved
 0010 = Compare mode, toggle output on match
 0011 = Capture mode
 0100 = Capture mode, every falling edge
 0101 = Capture mode, every rising edge
 0110 = Capture mode, every 4th rising edge
 0111 = Capture mode, every 16th rising edge
 1000 = Compare mode, initialize CCP1 pin low, set output on compare match (set CCP1IF)
 1001 = Compare mode, initialize CCP1 pin high, clear output on compare match (set CCP1IF)
 1010 = Compare mode, generate software interrupt only, CCP1 pin reverts to I/O state
 1011 = Compare mode, trigger special event (CCP1 resets TMR1 or TMR3, sets CCP1IF bit)
 1100 = PWM mode: P1A, P1C active-high; P1B, P1D active-high
 1101 = PWM mode: P1A, P1C active-high; P1B, P1D active-low
 1110 = PWM mode: P1A, P1C active-low; P1B, P1D active-high
 1111 = PWM mode: P1A, P1C active-low; P1B, P1D active-low

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APPENDIX IX : RECEIVE STATUS AND CONTROL REGISTER (RCSTA)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R-0	R-0	R-x
SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

- bit 7 **SPEN:** Serial Port Enable bit
 1 = Serial port enabled (configures RX/DT and TX/CK pins as serial port pins)
 0 = Serial port disabled (held in Reset)
- bit 6 **RX9:** 9-Bit Receive Enable bit
 1 = Selects 9-bit reception
 0 = Selects 8-bit reception
- bit 5 **SREN:** Single Receive Enable bit
Asynchronous mode:
 Don't care.
Synchronous mode – Master:
 1 = Enables single receive
 0 = Disables single receive
 This bit is cleared after reception is complete.
Synchronous mode – Slave:
 Don't care.
- bit 4 **CREN:** Continuous Receive Enable bit
Asynchronous mode:
 1 = Enables receiver
 0 = Disables receiver
Synchronous mode:
 1 = Enables continuous receive until enable bit CREN is cleared (CREN overrides SREN)
 0 = Disables continuous receive
- bit 3 **ADDEN:** Address Detect Enable bit
Asynchronous mode 9-bit (RX9 = 1):
 1 = Enables address detection, enables interrupt and loads the receive buffer when RSR<8> is set
 0 = Disables address detection, all bytes are received and ninth bit can be used as parity bit
Asynchronous mode 8-bit (RX9 = 0):
 Don't care.
- bit 2 **FERR:** Framing Error bit
 1 = Framing error (can be updated by reading RCREG register and receiving next valid byte)
 0 = No framing error
- bit 1 **OERR:** Overrun Error bit
 1 = Overrun error (can be cleared by clearing bit CREN)
 0 = No overrun error
- bit 0 **RX9D:** 9th bit of Received Data
 This can be address/data bit or a parity bit and must be calculated by user firmware.



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APPENDIX X : BAUD RATE CONTROL REGISTER (BAUDCON)

R/W-0	R-1	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0
ABDOVF	RCIDL	RXDTP	TXCKP	BRG16	—	WUE	ABDEN
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Dit is set	'0' = Dit is cleared	x = Dit is unknown

- bit 7 **ABDOVF:** Auto-Baud Acquisition Rollover Status bit
 1 = A BRG rollover has occurred during Auto-Baud Rate Detect mode (must be cleared in software)
 0 = No BRG rollover has occurred
- bit 6 **RCIDL:** Receive Operation Idle Status bit
 1 = Receive operation is Idle
 0 = Receive operation is active
- bit 5 **RXDTP:** Received Data Polarity Select bit
Asynchronous mode:
 1 = RX data is inverted
 0 = RX data received is not inverted
Synchronous modes:
 1 = Received Data (DT) is inverted. Idle state is a low level.
 0 = No inversion of Data (DT). Idle state is a high level.
- bit 4 **TXCKP:** Clock and Data Polarity Select bit
Asynchronous mode:
 1 = TX data is inverted
 0 = TX data is not inverted
Synchronous modes:
 1 = Clock (CK) is inverted. Idle state is a high level.
 0 = No inversion of Clock (CK). Idle state is a low level.
- bit 3 **BRG16:** 16-Bit Baud Rate Register Enable bit
 1 = 16-bit Baud Rate Generator – SPBRGH and SPBRG
 0 = 8-bit Baud Rate Generator – SPBRG only (Compatible mode), SPBRGH value ignored
- bit 2 **Unimplemented:** Read as '0'
- bit 1 **WUE:** Wake-up Enable bit
Asynchronous mode:
 1 = EUSART will continue to sample the RX pin – interrupt generated on falling edge; bit cleared in hardware on following rising edge
 0 = RX pin not monitored or rising edge detected
Synchronous mode:
 Unused in this mode.
- bit 0 **ABDEN:** Auto-Baud Detect Enable bit
Asynchronous mode:
 1 = Enable baud rate measurement on the next character. Requires reception of a Sync field (55h); cleared in hardware upon completion.
 0 = Baud rate measurement disabled or completed
Synchronous mode:
 Unused in this mode.

