UNIVERSITI TUN HUSSEIN ONN MALAYSIA

FINAL EXAMINATION
SEMESTER II
SESSION 2012/2013

COURSE NAME	:	DIGITAL ELECTRONICS
COURSE CODE	:	DAE 21203
PROGRAMME	:	2 DAE
EXAMINATION DATE	:	MARCH 2013
DURATION	:	2 ½ HOURS
INSTRUCTIONS	:	ANSWER **FOUR (4)** QUESTIONS ONLY

THIS QUESTION PAPER CONSISTS OF EIGHT (8) PAGES

Q1 (a) Perform the following arithmetic operation. Show all your steps:

(i) $18_{10} - 25_{10}$ using 2's complement.
(ii) $93_{BCD} + 15_{BCD}$.
(iii) Signed binary numbers: 11101101 + 00001100. Give answer in decimal number.

(9 marks)

(b) Convert $3B9_{HEX}$ to base 2, 8 and 10 number systems.

(5 marks)

(c) Encode "A = 38/x" in ASCII code (excluding the quotes) using odd parity. The ASCII table is given in Table Q1(c).

(8 marks)

(d) A computer has a word length of 8 bits (including sign bit). If TWO's complement is used to represent negative numbers, what range of integers can be stored in the computer?

(3 marks)

Q2 (a) (i) Write the equations for DeMorgan's theorem.
(ii) Use basic gates to illustrate the two DeMorgan's theorems
(iii) Write the output expression for each gate.

(6 marks)

(b) A technician needs an AND gate to complete a design, but only NOR gates are available. Show how NOR gates can be used to implement an AND gate.

(2 marks)

(c) Simplify F using Boolean algebra laws for the following function:

$$F = A\overline{B}C + ABC + (C + D)(\overline{D} + E)$$

(4 marks)

(d) Waveforms A, B and C of Figure Q2(d) are applied to a logic circuit. The output waveform, D, from the circuit is also shown in Figure Q2(d). Obtain the truth table and Boolean expression of the logic circuit. Simplify the expression for D and implement with NAND gates only.

(13 marks)

Q3 (a) For the following function:

(i) Simplify using a Karnaugh map and obtain a minimum SOP expression for *f*.
(ii) Implement the simplified logic diagram using logic gates.

$$f(A,B,C,D) = \sum m\ (2,3,6,9) + d(10,11,12,13,14,15)$$

(9 marks)

(b) A combinational circuit has 4 inputs (A, B, C, D) and 3 outputs (X, Y, Z). X, Y, Z represent a binary number whose value equals the number of 1's at the input. For example, if ABCD = 1011, XYZ = 011. Find the

(i) Obtain the truth table of the circuit.
(ii) Write the minterm expression for outputs X, Y, and Z.
(iii) Write the maxterm expression for outputs X, Y, and Z.
(iv) Simplify the output function for X, Y, and Z.

(16 marks)

Q4 (a) From the truth table in Table Q4(a),

(i) Write the standard sum of product (SOP) expression for output P.
(ii) Write the standard product of sum (POS) expression for P
(iii) Use the K map to get the minimum sum of product (SOP) expression for P.
(iv) Implement the simplified expression of P with logic gates.

(11 marks)

(b) For the logic circuit shown in Figure Q4(b)

(i) Construct the truth table
(ii) Write the output expression.

(5 marks)

(c) Represent each function below as a sum of minterms:

(i) $F = \overline{A}B + \overline{A}C + A\overline{B} + \overline{B}C$

(ii) $F = \overline{X}\overline{Z} + W\overline{X}\overline{Y} + \overline{W}XZ$

(9 marks)

Q5. (a) A full adder can be implemented in many different ways. Figure Q5(a) shows how one may be constructed from 2 Half Adders. Construct a truth table for this arrangement and verify that it operates as a Full Adder.

(10 marks)

(b) Figure Q5(b) show a BCD adder circuit.

(i) What are the THREE basic parts of this adder?
(ii) Describe how the BCD adder circuit detects the need for a correction and executes it.
(iii) Write the expression for X.
(iv) Two numbers, A and B having values 9 and 5 respectively are feed into this BCD adder. Show the contents of $A_3A_2A_1A_0$, $B_3B_2B_1B_0$, $S_3S_2S_1S_0$, $\sum_3\sum_2\sum_1\sum_0$ and the value of X. Verify that the contents of the BCD sum and value of X is correct.

(15 marks)

Q6. (a) With the aid of diagrams, explain the function of the following devices:

(i) A decoder
(ii) An encoder
(iii) A multiplexer

(9 marks)

(b) For the circuit in Figure Q6(b),

(i) Construct the truth table
(ii) Write the expression for outputs $\sum$ and Co in sum of minterms.
(iii) Use a 3 x 8 decoder with active Low output and appropriate logic gates to implement $\sum$ and Co.

(11 marks)

(c) Implement this circuit using a 8 x 1 multiplexer to produce the Boolean expression:

$Z = A\overline{B}C + AB\overline{C} + BC$

(5 marks)

- END OF QUESTION -

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Table Q1(c)

CONTROL CHARACTERS				GRAPHIC SYMBOLS											
NAME	DEC	BINARY	HEX	SYMBOL	DEC	BINARY	HEX	SYMBOL	DEC	BINARY	HEX	SYMBOL	DEC	BINARY	HEX
NUL	0	0000000	00	space	32	0100000	20	@	64	1000000	40	`	96	1100000	60
SOH	1	0000001	01	!	33	0100001	21	A	65	1000001	41	a	97	1100001	61
STX	2	0000010	02	"	34	0100010	22	B	66	1000010	42	b	98	1100010	62
ETX	3	0000011	03	#	35	0100011	23	C	67	1000011	43	c	99	1100011	63
EOT	4	0000100	04	$	36	0100100	24	D	68	1000100	44	d	100	1100100	64
ENQ	5	0000101	05	%	37	0100101	25	E	69	1000101	45	e	101	1100101	65
ACK	6	0000110	06	&	38	0100110	26	F	70	1000110	46	f	102	1100110	66
BEL	7	0000111	07	'	39	0100111	27	G	71	1000111	47	g	103	1100111	67
BS	8	0001000	08	(	40	0101000	28	H	72	1001000	48	h	104	1101000	68
HT	9	0001001	09	)	41	0101001	29	I	73	1001001	49	i	105	1101001	69
LF	10	0001010	0A	*	42	0101010	2A	J	74	1001010	4A	j	106	1101010	6A
VT	11	0001011	0B	+	43	0101011	2B	K	75	1001011	4B	k	107	1101011	6B
FF	12	0001100	0C	,	44	0101100	2C	L	76	1001100	4C	l	108	1101100	6C
CR	13	0001101	0D	–	45	0101101	2D	M	77	1001101	4D	m	109	1101101	6D
SO	14	0001110	0E	.	46	0101110	2E	N	78	1001110	4E	n	110	1101110	6E
SI	15	0001111	0F	/	47	0101111	2F	O	79	1001111	4F	o	111	1101111	6F
DLE	16	0010000	10	0	48	0110000	30	P	80	1010000	50	p	112	1110000	70
DC1	17	0010001	11	1	49	0110001	31	Q	81	1010001	51	q	113	1110001	71
DC2	18	0010010	12	2	50	0110010	32	R	82	1010010	52	r	114	1110010	72
DC3	19	0010011	13	3	51	0110011	33	S	83	1010011	53	s	115	1110011	73
DC4	20	0010100	14	4	52	0110100	34	T	84	1010100	54	t	116	1110100	74
NAK	21	0010101	15	5	53	0110101	35	U	85	1010101	55	u	117	1110101	75
SYN	22	0010110	16	6	54	0110110	36	V	86	1010110	56	v	118	1110110	76
ETB	23	0010111	17	7	55	0110111	37	W	87	1010111	57	w	119	1110111	77
CAN	24	0011000	18	8	56	0111000	38	X	88	1011000	58	x	120	1111000	78
EM	25	0011001	19	9	57	0111001	39	Y	89	1011001	59	y	121	1111001	79
SUB	26	0011010	1A	:	58	0111010	3A	Z	90	1011010	5A	z	122	1111010	7A
ESC	27	0011011	1B	;	59	0111011	3B	[	91	1011011	5B	{	123	1111011	7B
FS	28	0011100	1C	<	60	0111100	3C	\	92	1011100	5C	|	124	1111100	7C
GS	29	0011101	1D	=	61	0111101	3D	]	93	1011101	5D	}	125	1111101	7D
RS	30	0011110	1E	>	62	0111110	3E	^	94	1011110	5E	~	126	1111110	7E
US	31	0011111	1F	?	63	0111111	3F	_	95	1011111	5F	Del	127	1111111	7F

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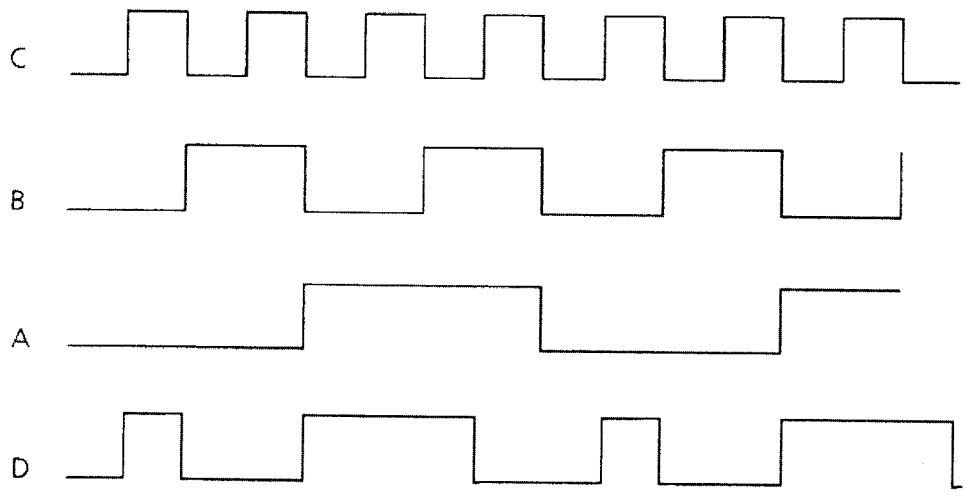

FIGURE Q2(d)

TABLE Q4(a)

INPUT			OUTPUT
A	B	C	P
0	0	0	1
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

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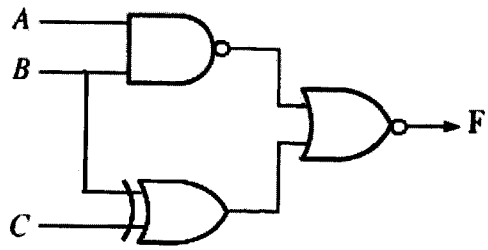

FIGURE Q4(b)

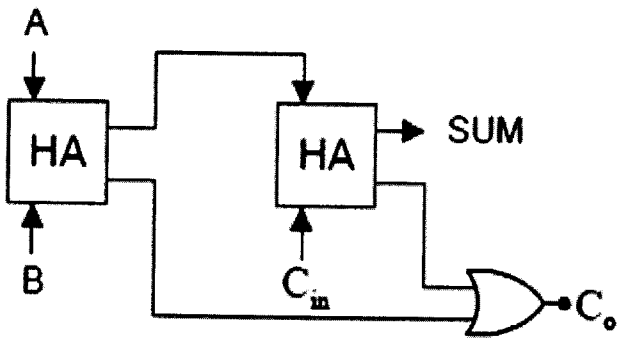

FIGURE Q5(a)

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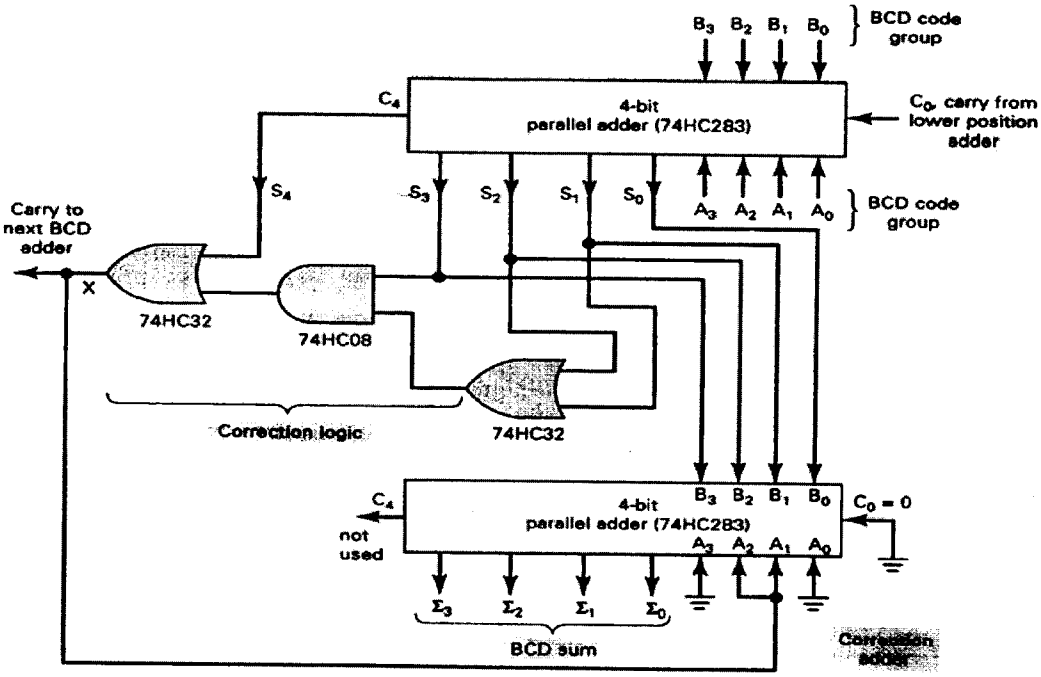

FIGURE Q5(b)

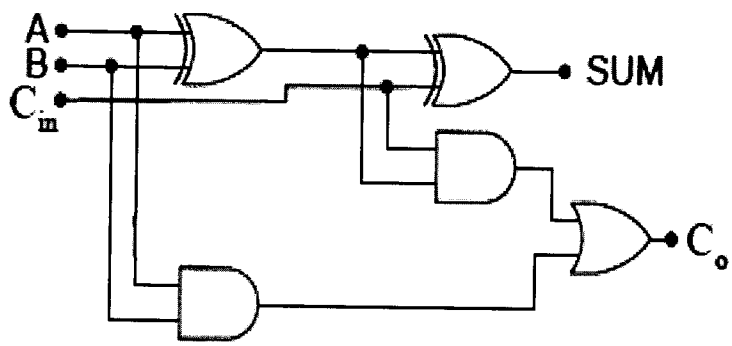

FIGURE Q6(b)